

AMPEX

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1 System Features and Functions

The UNIX PC is an intelligent desktop workstation that provides users with personal computing and enhanced voice and data communications services. It provides the UNIX System V virtual memory operating system in a telephone network environment. The UNIX PC can connect to a telephone system to allow communication with other telephones, workstations, and computers. Direct connection, or connection through a local area network, to other terminals, workstations, or computers, is also provided. The UNIX PC can be upgraded to a multiuser system.

The UNIX PC consists of the following parts, as illustrated in Figure 1-1:

- o Base unit
- o Keyboard
- o Mouse

The workstation base unit houses the monitor, power supply, hard disk drive, floppy disk drive, logic board, and three expansion slots. The logic board provides the processor logic, bit-mapped graphics logic, communications, and interface logic for all connected input/output (I/O) devices. The monitor is attached to a base that allows it to tilt and swivel.

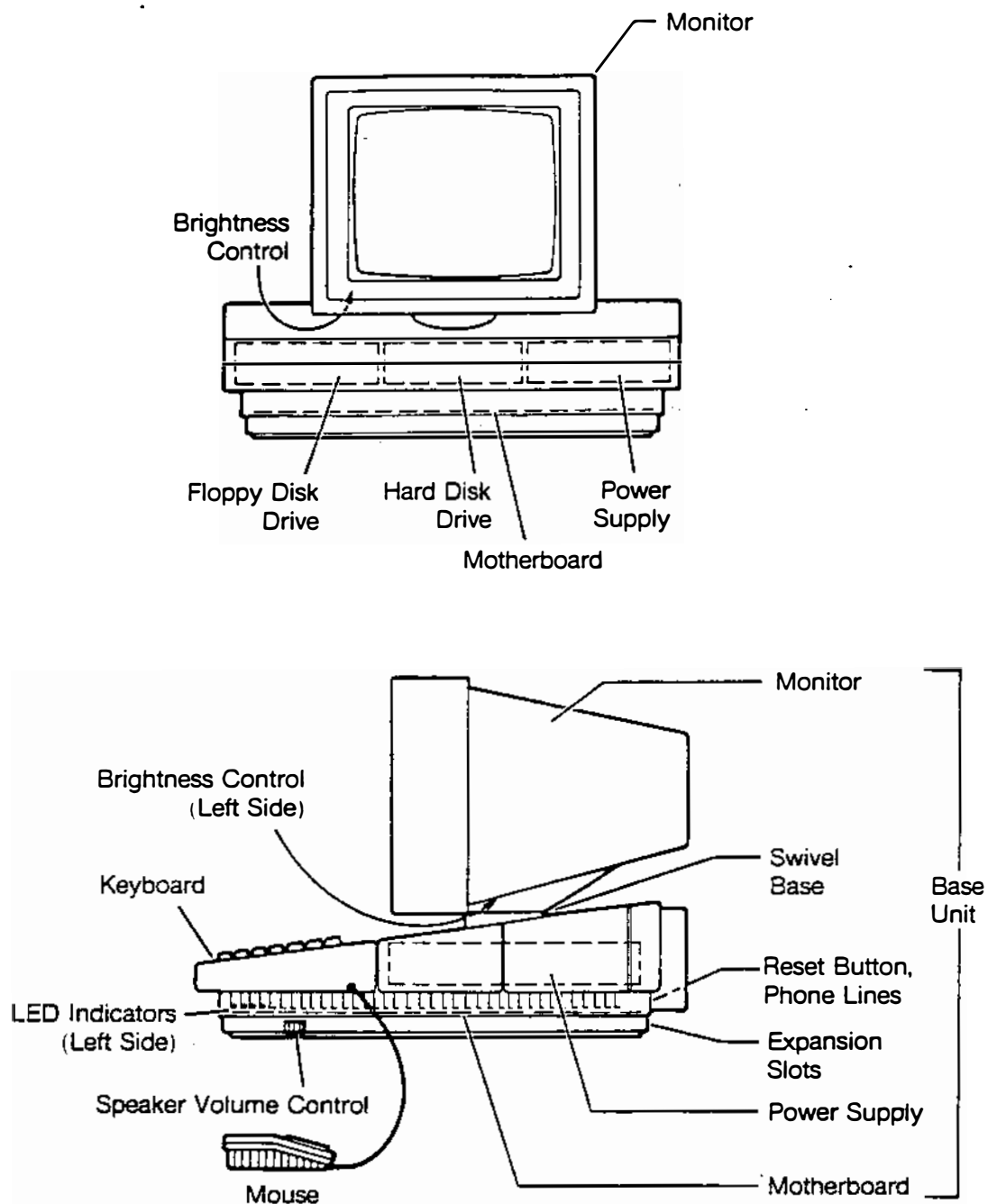


Figure 1-1 Base Unit, Keyboard, and Mouse

Functional Specifications

These specifications describe the major circuitry general characteristics of the UNIX PC system.

Logic Board

The Logic Board is shown in Figure 1-4.

- o Motorola 68010 central processing unit (CPU) with 10-megahertz (MHz) clock.
- o Virtual memory address of 4 megabytes (MB).
- o 1 MB standard or 2 MB random access memory (RAM).
- o 720 by 348 bit-mapped graphics monitor interface.
- o DTE RS-232-C serial port.
- o Centronics-compatible parallel printer port.
- o Keyboard interface.
- o Telephone interfaces for voice and data service. Three modular jacks are used: one for connection to a user-provided telephone and the other two for connection to tip/ring telephone lines. Also included is an integrated 300/1200 bits per second (bps) modem compatible with AT&T Models 103 and 212, offering asynchronous operation and autobaud capabilities.
- o Hard disk interface.
- o Floppy disk interface.
- o Expansion bus interface that allows memory and I/O expansion. The bus has 21 address lines and 16 data lines and will support bus mastership by expansion hardware.
- o A realtime clock that retains the time and date when the UNIX PC is powered down.

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Terminal Subsystem

The monitor contains a 12-inch cathode ray tube (CRT), a deflection board, and a yoke. It provides a 20-MHz screen capable of displaying 720 by 348 pixels. The display can be programmed either as light on dark (normal) or dark on light (inverse video).

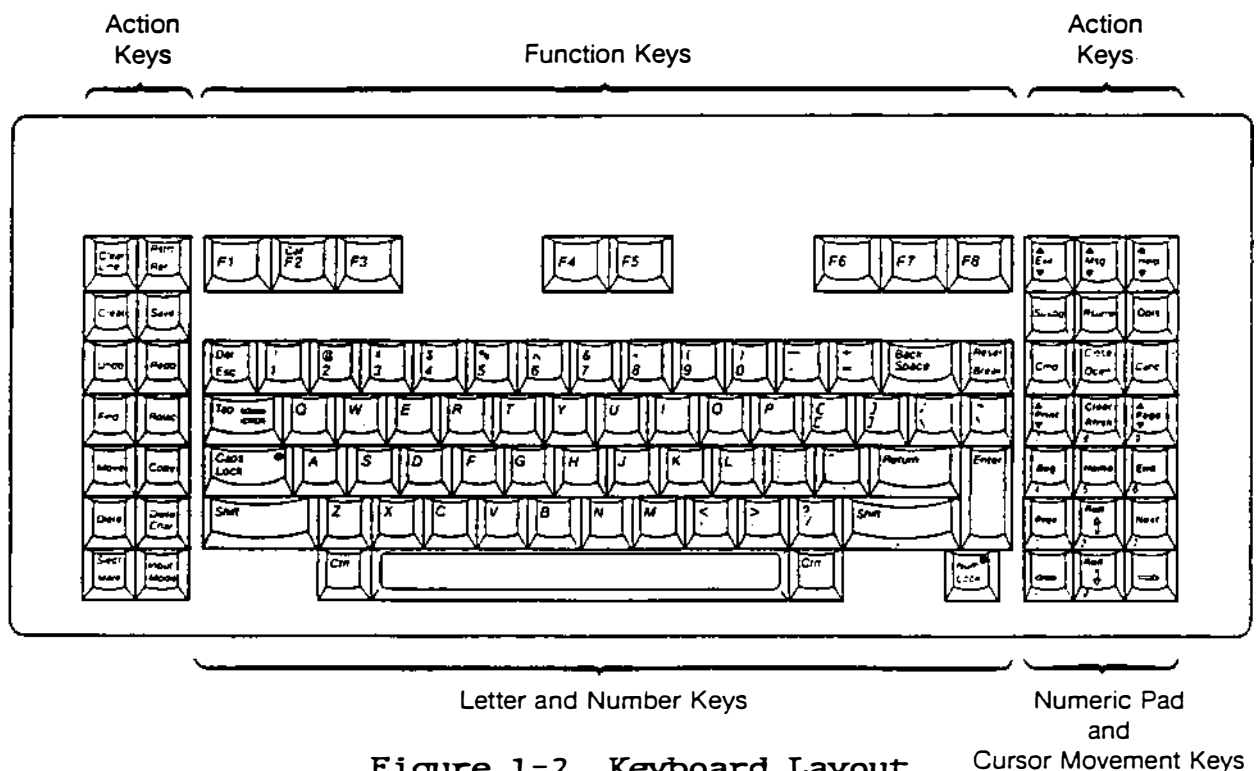
The monitor is attached to the base. The monitor can tilt -5 to +20 degrees relative to the horizontal plane and will swivel.

The screen is treated to reduce glare. A brightness control is accessible to the operator, as shown in Figure 1-1.

Keyboard

The keyboard is shown in Figure 1-2.

The keyboard is connected to the base with a flexible, coiled cord that can expand to approximately six feet. One end of the cord has about an inch of straight cord that plugs into the base unit. Both ends of the cable have connectors that prevent accidental disconnection.



Mouse

The mouse connects to the keyboard unit with a lightweight, uncoiled cord that is approximately four feet long. The cable has a connector that locks preventing accidental disconnection. The cord plugs into the keyboard. These connections are shown in Figure 1-3.

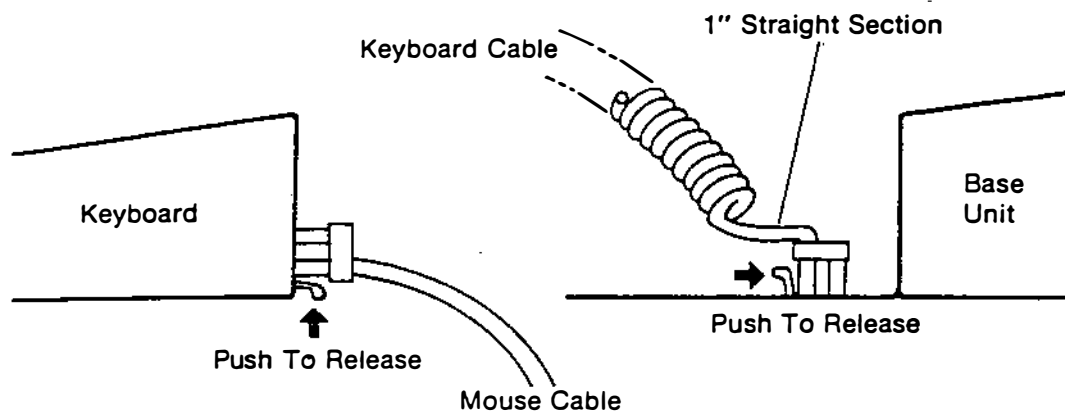


Figure 1-3 Keyboard and Mouse Connections

Audible Indicator

An audible indicator consisting of a small speaker is provided for monitoring telephone calls when using the Telephone Manager. A user-accessible slide volume control, illustrated in Figure 1-1, is located just under the right edge of the base unit.

Data Storage

Data may be stored either on a hard disk which is part of the UNIX PC system, or on floppy disks via the floppy disk drive. The storage capacities available are:

- o A 10MB, 20MB, 40MB or 67MB hard disk (Winchester) for mass storage

System Features and Functions

- o A double-sided, 1/2-MB, 5 1/4-inch, 48-tpi floppy disk drive.

RS-232-C Port

The RS-232-C port supports both synchronous and asynchronous data communications. Asynchronous bit rates of 110 bps to 19.2 Kbps are available.

RS-232-C Signals

The following table of signals applies to the RS-232-C connector. The table gives the pin number, signal name, and direction for the UNIX PC.

Table 1-1 RS-232-C Signals

Pin	Name	Direction
1	Ground (shield)	Bidirectional
2	Transmit data	Output
3	Receive data	Input
4	Request to send	Output
5	Clear to send	Input
6	Data set ready	Input
7	Ground	Bidirectional
8	Carrier detect	Input
15	Transmit clock	Input
17	Receive clock	Input
20	Data terminal ready	Output
22	Ring indicator	Input
24	DTE transmit clock	Output

Channel B of the 8274/7201 multiple protocol serial controller is connected to the modem. The following list describes the channel B signals:

8274/7201 Carrier detect <---RS-232-C ring indicator

8274/7201 Receive clock <----Modem receive clock

8274/7201 Clear to send <----RS-232-C data set ready

8274/7201 Transmit data----> Modem transmit data

8274/7201 Transmit clock <---Modem transmit clock

8274/7201 Receive data <-----Modem receive data

RS-232-C Signal Levels

Figure 1-4 illustrates the possible RS-232-C cabling to a printer or terminal.

Active data and clock signals produce -12V on the line and control signals produce +12V when active.

UNIX PC to Terminal Cable Pinning

<u>UNIX PC</u>	<u>Terminal</u>
1 -----	1
2 ----->	3
3 <-----	2
4-5-6	4-5-6
7 -----	7
8 ----->	20
20 <-----	8

UNIX PC to Printer with CTS Control

<u>UNIX PC</u>	<u>Printer</u>
1 -----	1
2 ----->	3
3 <-----	2
4 -----	4
5 <-----	5
6-8-20	
5 -----	7

Figure 1-4 RS-232-C Cabling

System Features and Functions

Diagnostic Loopback Plug

The diagnostic floppy tests RS-232-C functions through the use of a loopback plug, which must be installed when a channel is being tested.

Loopback plug (male) pinning is shown in Figure 1-5.

2	----->	3
4	----->	5
4	----->	8
20	----->	6
20	----->	22

(2) Transmit data -----	(3) Receive data
(4) Request to send -----	(5) Clear to send
(4) Request to send -----	(8) Carrier detect
(20) Data terminal ready ----	(6) Data set ready
(20) Data terminal ready ----	(22) Ring indicator

Figure 1-5 Loopback Plug Pinning

Centronics Parallel Printer Interface

Cable Pinning

Table 1-2 is an example of how a parallel printer cable might be constructed. The UNIX PC has an Amphenol 57 series 36-pin connector. This is a standard Centronics connector. The following guidelines do not have to be adhered to strictly when building your own cable (in the case of signal ground). Signal ground is tied to pins 16, 19, 30, and 33 on the UNIX PC connector.

Make sure your printer is strapped for negative strobes and acknowledges. Do not let any signals float. For example, if you are not going to use BUSY+, ground it.

This table shows typical pin functions for the Centronics printer cable:

Table 1-2 The Parallel Interface

Signal Pin	Return Pin	Signal	Direction	Description
1	19	<u>STROBE</u>	OUT	Pulse to read data in. Pulse width must be more than 0.5 ms at the receiving terminal.
2	20	DATA 1	OUT	These signals represent information of the 1st to 8th bits of parallel data, respectively. Each signal is at HIGH level when data is logical 1 and LOW when it is logical 0.
3	21	DATA 2	OUT	
4	22	DATA 3	OUT	
5	23	DATA 4	OUT	
6	24	DATA 5	OUT	
7	25	DATA 6	OUT	
8	26	DATA 7	OUT	
9	27	DATA 8	OUT	
10	28	<u>ACKNLG</u>	IN	Approximately 12-microsecond pulse. LOW indicates that data has been received and that the printer is ready to accept more data.
11	29	BUSY	IN	A HIGH signal indicates that the printer cannot receive data. The signal goes HIGH in the following cases: - o During data entry - o During printing - o When offline - o During printer-error state.
12	30	PE	IN	A HIGH signal indicates that the printer is out of paper.
13	--	LP SELECT	--	Pulled up to +5 volts through 3.3K-ohm resistance.

System Features and Functions

Table 1-2 The Parallel Interface (Continued)

Signal Pin	Return Pin	Signal	Direction	Description
14	--	AUTO FEED XT	--	When this signal is LOW, the paper is fed automatically one line after printing.
15	--	NC	--	Unused.
16	--	OV	--	Logic ground level.
17	--	CHASSIS GND	--	Printer's chassis ground, which is isolated from the logic ground.
18	--	NC	--	Unused.
19-30	--	GND	--	Twisted-pair return signal ground level.
31	--	INIT	OUT	When this level becomes LOW, the printer controller is reset to its initial state and the print buffer is cleared. This level is usually HIGH; its pulse width must be more than 50 ms at the receiving terminal.
32	--	ERROR	IN	This level becomes LOW when the printer is in: o Paper-end state o Offline o Error state.
33	--	GND	--	Same as for pins 19-30.
34	--	NC	--	Unused.
35	--	--	--	Pulled up to +5V through 3.3K-ohm resistance.

Table 1-2 The Parallel Interface (Continued)

Signal Pin	Return Pin	Signal	Direction	Description
38	--	SLCT IN	OUT	Data entry to the printer is possible only when this level is LOW.

Notes

- o The column heading "Return" denotes the twisted-pair return, to be connected at signal ground level. For the interface wiring, be sure to use a twisted-pair cable for each signal and to complete the connection on the return side. To prevent noise, these cables should be shielded and connected to the chassis of the host computer and the printer, respectively.
- o The column heading "Direction" refers to the direction of signal flow as viewed from the base unit.
- o All interface conditions are based on TTL level. The rise and fall times of each signal must be fewer than 0.2 microseconds.

Status Signal Description

- o LPNOPAPER+: Asserted by printer when paper-out sensor senses no paper in the printer.
- o LPBUSY+: Asserted by the printer to indicate that it cannot receive data. Also indicates a paper empty or fault condition.
- o LPSELECT+: Asserted by printer to indicate that it is selected and ready to receive data.
- o ERROR*: Asserted when there is a problem with the printer.

System Features and Functions

Expansion Slots

Three expansion slots are provided as part of the base unit. Expansion cards can be installed in any slot. However, depending on the memory being added, they must be located in accordance with the expansion memory location matrix in Appendix C.

Expansion slots support the seven different expansion boards listed below:

- o 0.5MB or 2MB expansion RAM board
- o Three versions of combo boards
 - 0.5MB or 1MB with two RS-232 ports
 - 0.5 MB without RS-232 ports
 - 1.5MB RAM expansion board
- o MS-DOS expansion board
- o Interface board for tape backup

Power is available for one memory expansion board, and an additional 3 amps per slot is provided for the other two expansion boards. A RAM expansion of 512 KB is available.

Physical and Electrical Specifications

The basic characteristics of the UNIX PC are:

- o Base unit: Approximately 20 inches wide, 18 inches deep, and 18 inches high; weighs approximately 40 pounds.
- o Keyboard: AT&T 103-key, low-profile design.
- o Electrical: 100-130 volts; maximum power under 400 watts.

Logic Board Bus System

This section describes the logic board bus system, including the address and data bus and the system control block diagram, which explains how bus transfers are regulated. Figure 1-6 shows the layout of the UNIX PC logic board.

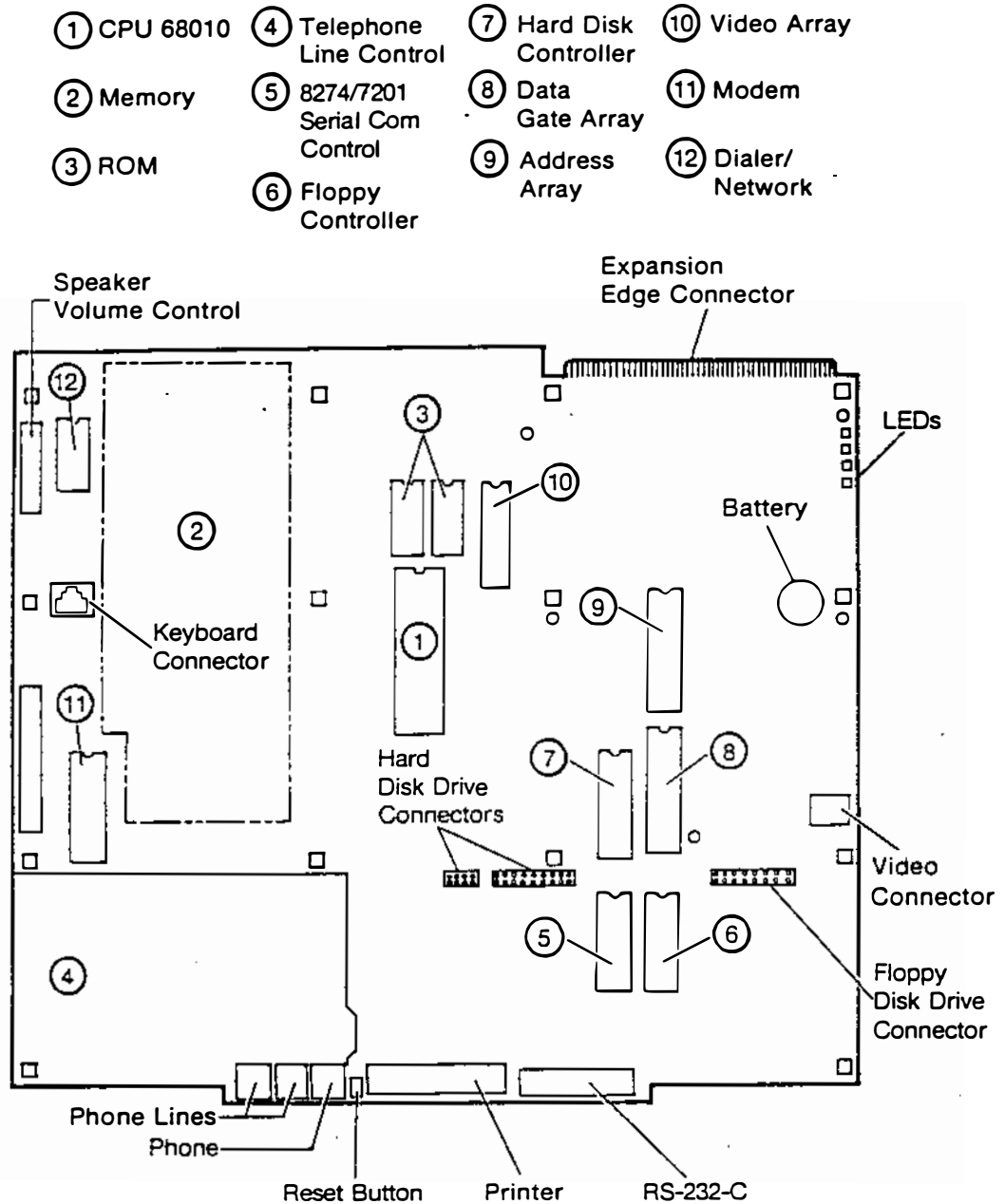


Figure 1-6 Logic board

Simplified Address and Data Block Diagram

The system block diagram in Figure 1-7 shows how the system bus allows the various devices within the UNIX PC CPU board to transmit data to each other.

The right half of the drawing shows the peripheral devices. Each peripheral has special control interface circuitry that modifies information coming from or going to the peripheral into a form that is acceptable for the bus and the peripheral. These circuits are indicated in the drawing by the rectangular boxes marked bit map, printer port, telephony controller, and so on. The bus accepts data 16 bits wide. The keyboard, for example, generates data in the form of a serial bit stream. These control interface circuits also receive control signals that initiate and terminate data transfers.

The left half of Figure 1-5 shows devices that do internal information processing. These include the 68010 CPU and the three forms of memory: ROM, RAM, and disk storage. The bus itself is really two buses, a data bus and an address bus.

The data bus consists of 16 wires, labeled D0-D15, for transmission of 16-bit data words. The address bus consists of 23 wires, labeled A1-A23. (There is an A0 function that is internal to 68010. From the programmer's point of view, the effect of the internal A0 is that all address references must be to even-numbered addresses because A0 is always 0.)

Data transfers on the UNIX PC bus are performed using a master-slave system. A master device such as the 68010 begins a transfer by first putting an address on the address bus to identify the device with which it will perform a data transfer. Then, depending on the direction of the data transfer, either master-to-slave or slave-to-master data is loaded onto the data bus, and the transfer takes place.

In the UNIX PC, the 68010 and the DMA (direct memory access) controller are both masters. There are other possible masters that are not shown for simplicity. Any of the devices on the right side of the drawing can be slaves to the 68010. The DMA controller for the disk drives transfers data only to RAM memory, so it has only one slave.

Before starting a DMA transfer, the 68010 must load information into the DMA controller, in which case the DMA controller is acting as a slave to the 68010. During the transfer, the DMA controller generates appropriate control signals that cause the transfer to begin and end and also determine the direction of the transfer, either from master to slave or slave to master. On the drawing, arrows indicate the direction of transfer. Notice that the address bus differs from the data bus in that the address bus allows only a one-way transfer of information, from master to slave. The data bus allows two-way transmission, as indicated by the arrows.

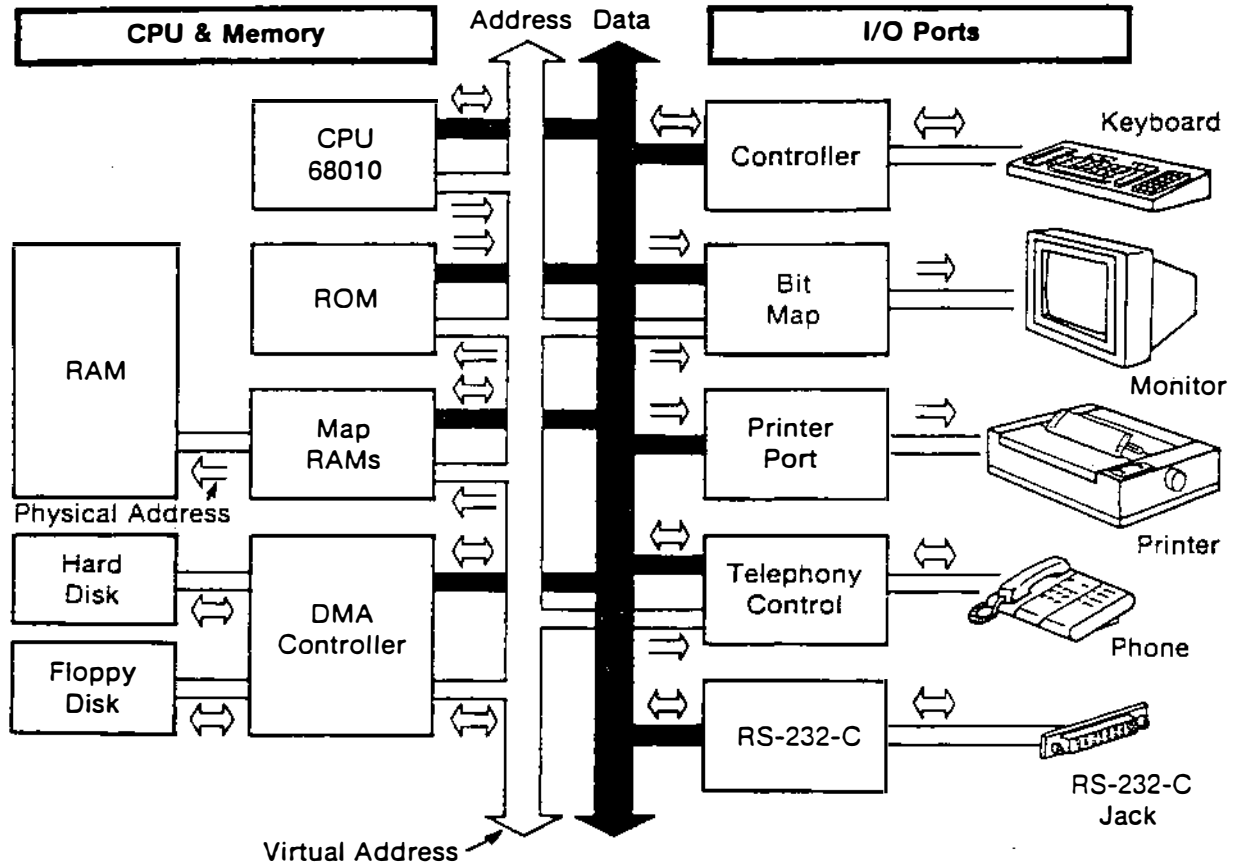


Figure 1-7 Bus System Block Diagram

System Features and Functions

Onboard Memory

Memory in the UNIX PC consists of both Random Access and Read Only memory, both are located on the logic board.

Random Access Memory

The logic board provides a minimum of 512 KB of onboard RAM, which can be expanded to 2 MB. A minimum memory configuration is made up of 72 type 4864, 64K by 1-bit dynamic RAM chips. The 1MB logic board is made up of 36 type 4256, 256K by 1 bit, 150ns, dynamic RAM chips. The 2MB logic board is made up of 72 type 4256, 256K by 1 bit, 150ns dynamic ram chips. The memory is used for program execution. It is organized into a virtual memory system, which allows the programmer to write programs as if there were a much larger amount of memory available than is physically present. The UNIX PC virtual memory system is 4 MB. The hardware provides this function through a special set of memory chips called page map RAM's. These RAM's are 1K by 4-bit static RAM chips. Video bit-map RAM is 32 KB.

Read Only Memory

The logic board contains two 2764 8-KB or two 27128 16-KB ROM chips. They hold the initialization program that is run when the power is turned on or the Reset button is pressed.

System Control Block Diagram

The system control block diagram, Figure 1-8, shows how the system determines which bus master controls the bus at any given time. There are three elements to system control: interrupt, memory management, and bus arbitration.

The right side of the drawing shows the I/O controller logic. When a peripheral device such as the keyboard wants to send data to the system, its controller sends an interrupt signal to the interrupt logic. This is one method of communication between an I/O device and the system.

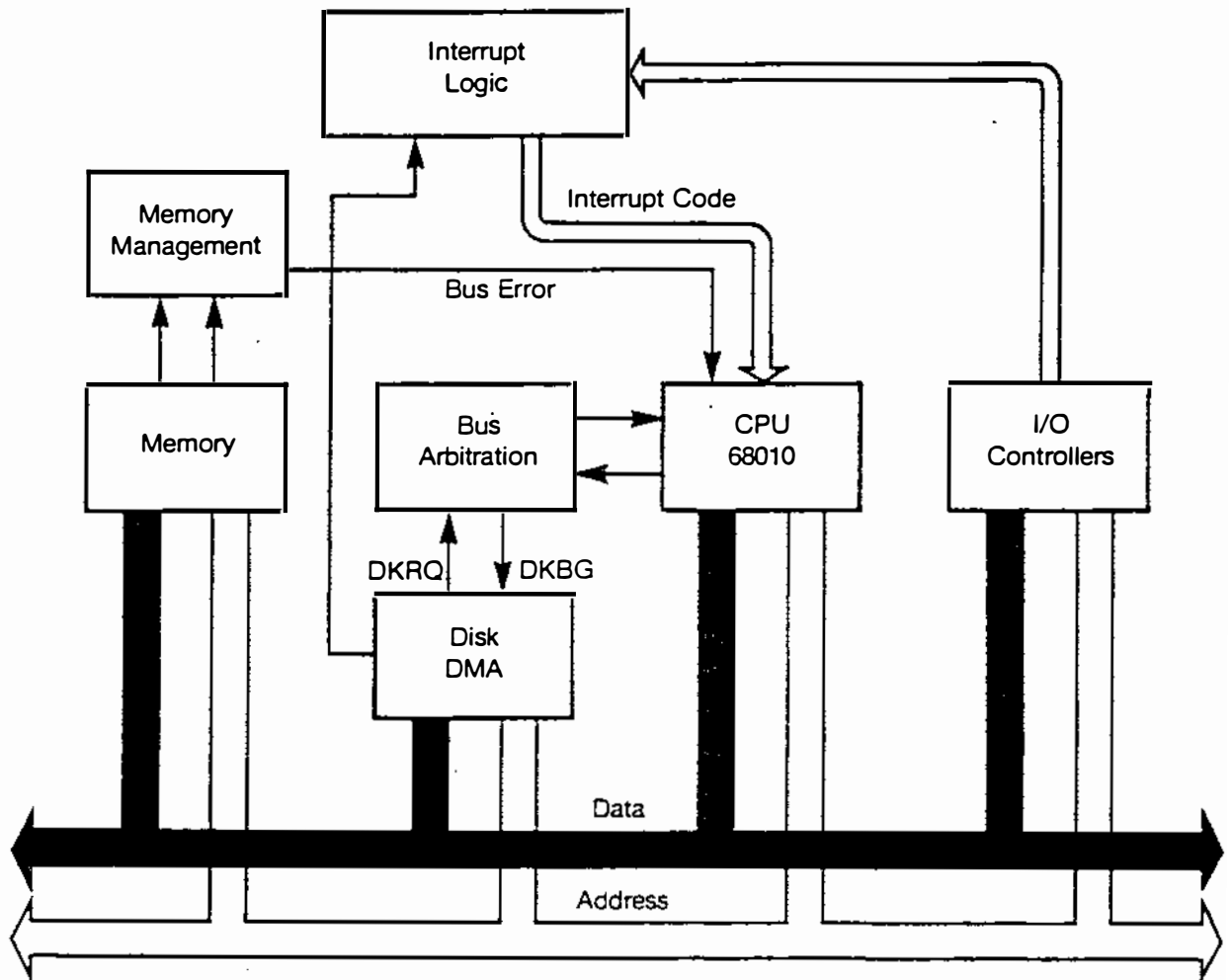


Figure 1-8 System Control Block Diagram

The interrupt signal is compared to a priority list. The highest priority pending at any given time causes the interrupt logic to send a signal to the 68010. The 68010 then responds by performing a sequence of data movements called an interrupt acknowledge. The function of the interrupt acknowledge is to allow the processor to store its current status so it can return to the same state after responding to the interrupt. First it completes execution of its current instruction and stores the status of its internal registers. Then it jumps to an interrupt service program that determines which device generated the interrupt. Finally, it jumps to a program to service that particular interrupt. Interrupt priorities are listed in Table 1-3.

Table 1-3 Interrupt Priorities

Priority Level	Device
7 (highest)	Parity error (logic board)
6	Video 60-Hz bit map (logic board)
5	Expansion slots 1, 2, and 3
4	274/7201 communication (detection circuit, RS-232-C)
3	Keyboard/mouse, modem
2	Hard disk drive, floppy disk drive, or line printer
1 (lowest)	Expansion slots 1, 2, and 3

Note: Levels 1 and 5 are available to expansion slots 1, 2, and 3.

Memory Management

A second element of system control is the memory management unit shown on the left in Figure 1-6. This unit monitors every access to the dynamic RAM memory chips. Certain accesses cause a memory management error. For example, if a user program attempts to write to a memory address that has been defined as being in disk space and not in physical RAM, the memory management unit generates a signal called a bus error. The 68010 then performs a data transfer with the disk DMA control unit. For this example, the disk is a slave and the 68010 is a master. The 68010 tells the disk DMA controller to do a transfer with the disk drives to correct the problem by moving data from disk storage to RAM. Then the 68010 starts performing other functions.

Bus Arbitration

At this point the two bus masters both want control of the bus. The third element of system control, the bus arbitration unit, resolves the conflict. It evaluates requests for bus control from masters and grants bus control on a priority basis. The 68010 has lower priority than the disk controller. The 68010 has to wait for the disk controller to release control of the bus before it can take control. When the disk controller is finished transferring data, it generates an interrupt to the interrupt logic. The interrupt logic then informs the 68010 that the transfer is complete. The 68010 resumes program execution at the point where it left off when the memory management unit generated the original interrupt.

Table 1-4 Bus Arbitration Priorities

<u>Priority Level</u>	<u>Device</u>
6 (highest)	Refresh
5	Expansion slot 1
4	Disk Interface Hard and Floppy
3	Expansion Slot 2
2	Expansion Slot 3
1 (lowest)	68010 CPU

2 Logic Board Theory of Operation

This overview summarizes the major functions performed by the logic board hardware. In addition, it describes the boot ROM program algorithm.

The logic board hardware functions include:

- o Direct memory access and bus arbitration
- o Machine cycle timing
- o Memory management
- o Input/output handling

Direct Memory Access

The UNIX PC bus is shared by the 68010 central processing unit (CPU) and several direct memory access (DMA) devices, such as the disk bus interface unit, dynamic RAM refresh, and expansion boards. During a DMA transfer, the 68010 waits while data is moved directly from a DMA device, such as the disk bus interface unit, into RAM memory. DMA provides high-speed transfer of blocks of data to or from memory.

Machine Cycle Timing

A 68010 machine cycle consists of putting an address on the bus, reading data, and disconnecting from the bus. Machine cycles are either fast (400 nanoseconds) or slow (1100 ns). Access to the lower half of the address space results in a fast cycle; access to the upper address space results in a slow cycle. DMA machine cycles are considered fast (500 ns).

Logic Board Theory of Operation

Memory Management

Programs run on the UNIX PC are often too large to fit in the RAM memory chips on the logic board. Thus, when the system is booted up, only a portion of the program is loaded into memory. While the program is being executed, it is monitored by memory management hardware. When a portion of the program that is on the disk is needed, the memory management hardware generates an error, causing the DMA to move the required portion of the program from the disk drive into RAM memory.

The processor can address locations anywhere in the entire 16 megabytes (MB) of system space, but the DMA can access only the lower 1/4 MB of virtual memory space that is used by RAM.

Input/Output Handling

Input and output (I/O) operations are memory mapped--that is, the 68010 does not have separate instructions for I/O operations. I/O ports are accessed by assigning addresses to them. I/O operations can be handled either by interrupt or by polling. Polling can be used in boot ROM programs where stack operations are forbidden to avoid using RAM memory. Table 2-1 lists the 68010 processor pin functions

Boot ROM Algorithm

The boot ROM program tests memory. It programs the initial status of the memory management hardware and various peripheral controller chips. Then it loads a program from floppy or hard disk and jumps to that program.

Table 2-1 68010 Processor Pin Functions

Pin No.	Description	Mnemonic
29-52	A01-A23	24-bit address bus (outputs only)--A unidirectional, three-state bus capable of addressing 16 MB of data. Provides addressing for all CPU cycles except space cycles.
1-5 54-64	D00-D15	16-bit data bus--Bidirectional, three-state bus that is the general purpose data path. Transfers either words or bytes.
6	AS	Address strobe--Signal indicating that there is a valid address on address bus 9 Read/Write Defines the data bus transfer as a read or write cycle.
7-8	UDS, LDS	Upper and lower data strobes--Signals used with R/W to control data flow on the data bus. UDS enables the upper byte; LDS enables the lower byte. When both are active, words are transferred.
10	<u>DTACK</u>	Data transfer acknowledge--Input indicating that a data transfer has been completed. When received during a read cycle, data is latched one clock cycle later and the bus cycle is terminated. When received during a write cycle, the bus cycle is terminated.
13	<u>BR</u>	Bus request--Not used
11	<u>BG</u>	Bus grant--Not used

Logic Board Theory of Operation

Table 2-1 68010 Processor Pin Functions (Continued)

Pin No.	Mnemonic	Description																																				
12	<u>BGACK</u>	Bus grant acknowledge--Not used																																				
23-25	<u>IPL0</u> , <u>IPL1</u> , <u>IPL2</u>	Interrupt priority level 0-2--Inputs indicating the encoded priority level of the device requesting to interrupt the CPU. Level 7 has highest priority, and level 0 indicates no interrupts present. Level 7 cannot be masked. These inputs must remain stable until the processor acknowledges, which is accomplished by setting FC0-FC2 and A04-A23 high.																																				
26-28	FC0, FC1, FC2	Function code 0-2--Outputs activated along with address strobe to indicate the state (user or supervisor) and the cycle type currently being executed. <table><tr><td><u>FC2</u></td><td><u>FC1</u></td><td><u>FC0</u></td><td><u>Cycle Type</u></td></tr><tr><td>Low</td><td>Low</td><td>Low</td><td>(Undefined)</td></tr><tr><td>Low</td><td>Low</td><td>High</td><td>User data</td></tr><tr><td>Low</td><td>High</td><td>Low</td><td>User program</td></tr><tr><td>Low</td><td>High</td><td>High</td><td>(Undefined)</td></tr><tr><td>High</td><td>Low</td><td>Low</td><td>(Undefined)</td></tr><tr><td>High</td><td>Low</td><td>High</td><td>Supervisor data</td></tr><tr><td>High</td><td>High</td><td>Low</td><td>Supervisor program</td></tr><tr><td>High</td><td>High</td><td>High</td><td>CPU space</td></tr></table>	<u>FC2</u>	<u>FC1</u>	<u>FC0</u>	<u>Cycle Type</u>	Low	Low	Low	(Undefined)	Low	Low	High	User data	Low	High	Low	User program	Low	High	High	(Undefined)	High	Low	Low	(Undefined)	High	Low	High	Supervisor data	High	High	Low	Supervisor program	High	High	High	CPU space
<u>FC2</u>	<u>FC1</u>	<u>FC0</u>	<u>Cycle Type</u>																																			
Low	Low	Low	(Undefined)																																			
Low	Low	High	User data																																			
Low	High	Low	User program																																			
Low	High	High	(Undefined)																																			
High	Low	Low	(Undefined)																																			
High	Low	High	Supervisor data																																			
High	High	Low	Supervisor program																																			
High	High	High	CPU space																																			
15	CLK	Clock--10-MHz input, internally buffered for development of timing needed internally by the processor.																																				
20	E	Enable--Not used																																				
19	VMA	Valid memory address--Not used																																				
21	<u>VPA</u>	Valid peripheral address--Asserted during an interrupt cycle to inform the CPU that the current interrupt cycle is an autovector cycle. As implemented in the UNIX PC, all interrupts are autovectored.																																				

Table 2-1 68010 Processor Pin Functions (Continued)

Pin No.	Mnemonic	Description
22	$\overline{\text{BERR}}$	Bus error--Input informing the CPU that there is a problem with the current cycle. Most commonly used when applied memory address is not in primary memory.
17	$\overline{\text{HALT}}$	Halt--Bidirectional. When used as input, the processor floats all outputs and stops at the completion of the current bus cycle. Other uses are described below.
18	$\overline{\text{RESET}}$	Reset--Bidirectional signal that resets the system upon power up or pressing the Reset button. The reset and halt inputs are tied together to ensure a total processor reset. Pressing the Reset button for 10 clock cycles causes a total system reset. Upon power up, reset and halt must be driven low for at least 100 ms. A software reset causes the reset signal to be driven for 124 clock cycles.

Note

An alphabetical listing of mnemonics used in this section appears in Appendix B.

Fast and Slow Cycles

68010 machine cycles are either fast (400 ns) or slow (1100 ns) depending on the address being accessed. The slow cycle is achieved by delaying the arrival of data transfer acknowledge to the 68010. A custom gate array circuit containing the timing circuit determines how much delay to provide through address decoding. DMA machine cycles are fast (500 ns) transfers between the DMA devices and RAM memory or refresh of RAM memory.

Table 2-2 shows how the two most significant address bits are decoded to select fast or slow cycles:

Table 2-2 Significant Address Decoding

A23	PA22	Region Description
0	0	RAM memory: fast-cycle access by 68010 user or supervisor mode
0	1	I/O registers: fast-cycle 68010 access in supervisor mode only
1	0	ROM memory: slow-cycle 68010 read in supervisor mode only
1	1	I/O registers: slow-cycle 68010 access in supervisor mode only

From the program execution viewpoint, fast and slow cycle transfers are identical. An instruction is executed in the same way except that the CPU waits for an acknowledge signal during slow-cycle transfers. After the read portion while doing the read-modify-write cycle, the CPU waits to allow any pending DMA requests to proceed. The CPU does the write portion when the system is idle.

The CPU adjusts the length of its machine cycle to meet the requirements of the bus. It drives address and control signals and waits for DTACK data transfer acknowledge (pin 10).

The 68010 is clocked by a 10-MHz signal called 1PCK. 1PCK is a 50% duty cycle clock with a full-cycle duration of 100 ns. The CPU uses four PCLK's to accomplish a fast bus cycle. These four clocks are broken into eight states (S0-S7) by the 68010:



The CPU samples DTACK* at the trailing edge of S4. If DTACK* is present at the trailing edge of S4, the processor verifies it at the leading edge of S5, latches data (for a read), tristates control signals at the trailing edge of S6, and tristates its address lines at the trailing edge of S7.

If DTACK* is not present, the processor begins inserting wait states and sampling DTACK* at the trailing edge of each succeeding PCLK. When DTACK* arrives, the processor behaves as described in the preceding paragraph. This describes the difference between a fast cycle and a slow cycle.

For a slow cycle, the hardware simply prevents the generation of DTACK* for an extra six clock cycles. The extra time is allotted for the slow response of the ROM and I/O devices.

68010 CPU machine cycles are either instruction fetches or instruction execution cycles. The 68010 outputs status bits that identify the type of cycle being performed. These status bits can be used by a logic analyzer to display only program execution to aid in troubleshooting.

Clock Generation

Sheet 3 refers to schematic sheet 3 in Chapter 5. Note that integrated circuits (IC) are referred to by their location identifiers. For example, 21F refers to an IC located at position 21F on the logic board. As seen from the front of the UNIX PC, parts on the logic board are identified with two coordinates. Numbers from left to right (1-28) and letters from front to back (A-P).

Logic Board Theory of Operation

System clock signals are generated as follows:

- o A 40-MHz oscillator provides the source frequency for the majority of the system clocks.
- o This frequency passes through OR gate 21F and provides the clock for dual J-K F/F 20G.
- o Pins 9 and 7 of 20G output a 20-MHz signal, and pins 5 and 6 output 10 MHz.
- o These signals are buffered at 19G and output as MCK and PCK.
- o 1PCK+ feeds the clock input of F/F 16K and causes the generation of the 5-MHz signal, 5MCK+.
- o 1PCK+ feeds the DMA address IC (22E, sheet 9) and causes the generation of the 1-MHz signal, 1MCK+.

Bus Arbitration

A bus arbitration programmable array logic (PAL) decides which DMA device accesses the bus when two DMA devices request the bus at the same time. When no DMA devices are requesting the bus, the 68010 controls the bus.

Bus Masters and Slaves

The UNIX PC uses a system address and data bus as shown in Figure 2-1. The system bus makes it possible for bus arbitration to switch the bus between several devices, called bus masters.

The devices connected to the system bus are classified as either bus masters or bus slaves. In every data transfer, one device is the master and one is the slave. The master outputs the control signal that starts the transfer and provides the address of the device to or from which it wants to transfer data. A bus slave is connected to the bus when an address decoder detects the presence of the address assigned to that device on the address bus.

Figure 2-1 shows two bus masters in the UNIX PC system, the 68010 CPU and the disk DMA controller, and a single device they can both transfer data to, the RAM memory array.

When the 68010 CPU transfers data to RAM memory, control signals are asserted that enable the tristate buffers and connect the 68010 address and data lines to the system address and data bus. At the same time, other control signals put the DMA circuits inside the custom DMA address and put data and gate array chips in a tristate condition, thus disconnecting them from the system address and data bus.

When the DMA gate array chips are transferring data between a disk drive and memory, the gate array address counter and data latch are enabled. The 68010 address and data buffers are in a tristate condition.

Logic Board Theory of Operation

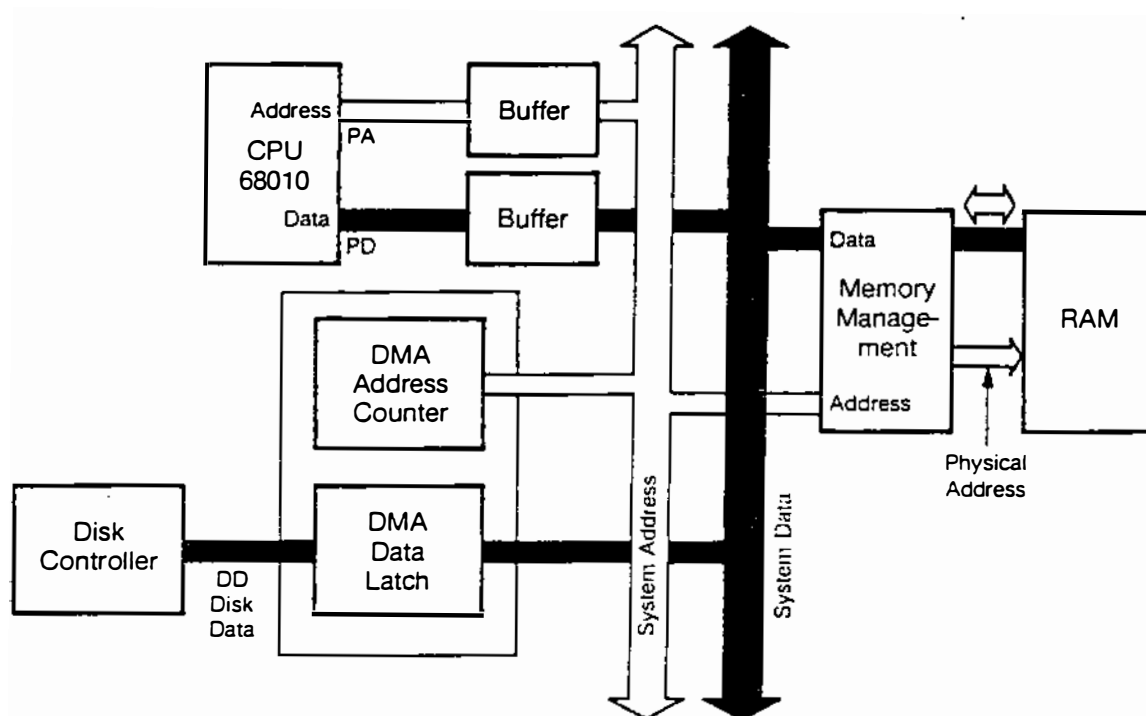


Figure 2-1 System Bus

Arbitration Priority

The process of deciding which bus master receives the bus at any given time is called bus arbitration. It takes place in the bus arbitration PAL shown on sheet 2 of the schematics. For a detailed discussion of PAL's, refer to Appendix A, PAL Equations.

The following table shows how priority is assigned to the various possible bus masters. With the exception of the processor, the other bus masters will be DMA. The 68010 issues no bus request; it is granted use of the system bus by default (no other requests are present).

Table 2-3 Bus Master Priorities

Priority	Bus Master
1	Disk bus interface unit
2	Expansion board 3
3	Refresh
4	Expansion board 2
5	Expansion board 1
6	Expansion board 0
7	68010

Arbitration Signal Sequence

When a bus master requires use of the system bus, it issues a bus request to the arbiter. If no higher priority requests are pending, the arbiter sends a bus grant to the requesting circuit.

The bus master then sends a bus grant acknowledge back to the arbiter, drops its request, and executes the bus cycle. The bus grant acknowledge latches the bus grant and locks out other requests.

When the bus cycle is finished, the bus master drops the bus grant acknowledge and the arbiter drops the grant.

The bus arbiter allows continuous transfers to occur. If another transfer is pending at the end of one transfer, the arbiter immediately sends a new bus grant and the next transfer begins.

Logic Board Theory of Operation

Memory: Theory of Operation

Onboard memory consists of random access memory (RAM). The logic board contains a minimum of 512K of RAM which may be expanded to 2 MB. The logic board also contains read-only memory (ROM) which holds the initialization program that is run when power is turned on or the Reset button is pressed.

Memory Address

The 68010 provides 24 address bits, although address bit 0 does not leave the CPU. This allows the addressing of 16 MB of memory. The data bus contains 16 bits. Memory operands can be either 8-bit bytes or 16-bit words.

All memory or register word accesses must be even-byte aligned. This means word instruction address operands must be even numbers. A0 is always zero. Address numbers are six hexadecimal digits from 000000 through FFFFFFFF. These correspond to 16 MB. Physical memory is organized in 16-bit words. The first word is address 000000, the second is 000002, the third is 000004, and so on. When even-numbered bytes are accessed, the upper half of the data bus D15 to D8 is used. When odd-numbered bytes are addressed, the lower half of the data bus, D7 to D0 is used. The internal address bit A0 is logically equivalent to the UDS (upper data strobe) pin of the 68010.

Words are accessed only at even addresses when both UDS and LDS are active.

Reset Vector Loading

When a system is powered or reset, the CPU automatically addresses ROM. A bootstrap routine directs the CPU to initialize the UNIX PC system and read the operating system from the disk.

When a system is reset, internal microcode forces the 68010 to read from RAM address 000000. Address 000000 is referred to as the reset vector. The 68010 loads the stack pointer with the values stored in addresses 000000 and 000002. It reads the values stored in addresses 000004 and 000006 and loads them into the program counter.

Actual address space for ROM is 800000-BFFFFFFF. The values necessary to initialize the stack pointer and the program counter are actually at addresses 800000 through 800006. Therefore, during a reset, the hardware is responsible for forcing address bit 23 high, thus causing the processor to refer to ROM.

During reset, a signal called ROMLMAP is generated and ORed with address bit 23. Although the processor is addressing 000000, ROMLMAP causes the address sent to ROM to be 800000.

At this point, the hardware forces the processor into the ROM address space, and no RAM references can be made as long as ROMLMAP is active. The boot code is responsible for vectoring the processor into legitimate ROM address space and must also cause the processor to deactivate ROMLMAP so RAM can be accessed again.

The processor is vectored into legitimate ROM address space by the first instruction executed after the program counter is loaded with the vector address at 800004 and 800006. This value is loaded into the program counter. The processor then fetches and begins instruction execution.

Now that the CPU is driving PA23 high, ROMLMAP is no longer necessary. In fact, it must be dropped to access RAM. The first instruction, addressed by the reset vector, causes 8000 to be written to address E43000. This deactivates ROMLMAP.

68010 ROM Read Sequence

The system must do a slow-cycle transfer to read ROM. The following description refers to the schematics in Chapter 5.

Sheet 5--Asserting reset:

- o Upon power up or depression of the Reset button, the HALT and RST pins of the 68010 are driven low by the power-up detection and reset switch debounce circuit.

Note

At power up, the RST and HALT pins must be low for a minimum of 100 ms. At reset, they must be low for 10 clock cycles.

- o At 60 ns after reset goes high, the CPU outputs the function code--in this case, FC2+, FC1+, and FC0- (supervisor program mode). The processor drives R/W* high (specifying a read operation) and places the address on the PA bus. Once the processor has been vectored into ROM, PA23 is a 1, and PA22 is a 0.

Logic Board Theory of Operation

Sheet 6--Asserting ROMLMAP*:

- o RST* clears the addressable latch 7K, causing the generation of ROMLMAP* from pin 7.

Sheet 5--Asserting SPA23 and PDS:

- o ROMLMAP* is inverted to a high by 3K. This is applied to gate 13E, which is logically equivalent to an OR gate. When it receives a high from 3K, it generates high output at SPA23.
- o At 120 ns the processor outputs AS*, UDS*, and LDS*. LDS* and UDS* generate PDS+.

Sheet 3--Asserting I/ORQ+:

- o PDS+, SPA23, and an inactive INTA* cause gate 27F to assert I/ORQ+.

Sheet 9--Asserting BGACK*:

- o I/ORQ+ causes the DMA address IC to assert BGACK*.

(This DMA address array is a custom gate array chip. In early versions of the UNIX PC logic boards, a piggyback gate array simulation board was used instead of gate array chips.)

Sheet 17--Asserting ROMEN:

- o 1 of 4 decoder 6J is enabled by BGACK* and addressed by SPA23 and PA22. SPA23 is high and PA22 is low, putting a binary 2 on the address inputs of the decoder. The decoder drives its Q2 output low, asserting ROMEN*.

Sheet 5--Addressing and enabling ROM:

- o BGC+ and MRAMEN* force the output of 25N (pin 11) low, enabling address buffers 16F and 17F. Transparent latch 17G is put into its transparent mode by gate 27H, pin 10 (MMUWREN+ and MMUWREND+), and the outputs are enabled by BGC+.
- o ROMEN* disables data transceivers 13C and 13D and enables boot ROM's 14C and 15C. Note that the ROM's output directly to the processor data bus.

- o At this point the boot ROM's are addressed, enabled, and asserting data; the processor has been inserting wait states, waiting for DTACK*. When DTACK* arrives, the processor latches the data on the trailing edge of the next PCK* and deasserts address and control signals.

Sheet 9--Disabling BGACK*:

- o 650 ns after I/ORQ+, the DMA address IC asserts I/O DTACK+; 900 ns after I/ORQ+, BGACK* is disabled.

Sheet 3--Asserting DTACK*:

- o I/O DTACK+ causes gate 27N to assert DTACK*.

Mapping Virtual Address

The memory management circuitry includes page status registers on sheet 16 and the memory management PAL on sheet 2. It performs four general functions:

- o Translates logical address to physical address
- o Updates the page status registers during each legal RAM access, either by the 68010 or DMA
- o If the access is illegal, inhibits the access and generates a memory management unit (MMU) error
- o Provides a data path for the 68010 to write page status to the page registers while servicing an interrupt resulting from an illegal access to RAM.

The address output of the 68010 and the DMA devices are virtual address. Virtual address space is fixed at 4 MB. Programs are assigned fixed positions within this large address space. This virtual memory is sectioned off into 1024 pages of equal length (4096 bytes), and the pages reside in either RAM (physical pages) or disk storage (logical pages). From any user program viewpoint, these pages are available storage, and a major task done by the supervisor program is to juggle pages between RAM memory on the logic board and the hard disk drive.

Logic Board Theory of Operation

The supervisor program uses map registers (static RAM chips) to locate pages in physical memory (RAM). The amount of physical address space can vary from 1MB to 3.5MB, depending on whether or not a memory expansion board is used. The map register's address input is a virtual or logical page address. Its data output lines are the physical page address plus status bits. These determine whether that page is located in the onboard RAM or in disk storage. There are 1024 map registers, one for each page of virtual memory.

When an instruction attempts to access a page that has been declared not present, the MMU PAL (memory management PAL, sheet 2) generates an error signal called PGF (page fault). This is used for internal processing and has priority over interrupts. To correct the page fault, a new page must be declared present. Since the number of pages that can be declared present is fixed, declaring a new page present means one that was present must be declared not present. The exception processing program determines which new page is declared present and which page that was present is declared not present. This determination is based on how long it has been since a given page was last accessed.

In real time, the computer can execute only one process at a time, at any given time, so the map registers contain page addresses pertaining to only one user's process. However, processes can share code or data, and each time the supervisor reloads the maps, it can load them so they point to both exclusive and shared memory.

Typically the kernel of the operating system is contained in the lowest portion of memory. This section of memory is unity mapped. Unity mapping means a one-to-one correspondence between virtual address into the map RAM's and physical address output. Virtual page 0 is mapped to physical page 0, virtual page 1 is mapped to physical page 1, and so on. The kernel is the lowest level of the operating system. It is responsible for scheduling processes, executing command sequences to peripheral controllers, and performing other similar tasks never seen by a user running an application program.

The process working set is the set of pages that currently resides in physical memory. Whenever the CPU reads or writes a memory location, the memory management hardware determines whether or not the page addressed is in the process working set. If it is not, the hardware generates a BERR CPU interrupt.

Upon receiving a BERR, the CPU invokes the supervisor. The supervisor sets up a DMA disk operation to obtain the missing page. Then it returns to CPU user mode, allowing it to do a different user process while the DMA is working. When the disk controller finishes the DMA operation, it interrupts the CPU. The supervisor notes the updated process working set and, either now or later, returns the CPU to the original user process.

The amount of physical memory determines the upper size limit of the process working set. As memory size increases, the upper size limit increases, which improves system performance by reducing disk transfers.

Virtual program memory is being addressed if address bits 22 and 23 are equal to 00. The memory control receives the lower 21 virtual address bits, via the logical address bus. The upper 10 bits (21-12) address the map logic to select a page. The maps output a 10-bit-mapped address, MA21-12, which, when combined with the lower 11 address bits (11-1), forms the complete physical memory address.

When a user loads an application program into the computer, the supervisor program sets up the map RAM's for that application, thus mapping the application onto an unused portion of memory. As the user inputs more information, the supervisor sends data back to the disk, remembering where it has sent the data and to which application it belongs.

During each memory access, the map logic updates a table, called the page map table, to indicate the result of the access. This table consists of two page status bits, which indicate the status for each page of memory as follows:

- o Not present (memory not installed at that address)
- o Present but not accessed
- o Accessed but not written to
- o Written (in this case, the information in this page of memory must be stored on disk before the page can be overwritten)

Map Addresses MA12-MA21

The page mapping RAM's (integrated circuits 19C through 22C) are shown on sheet 16.

Logic Board Theory of Operation

The page mapping RAM's receive 10 bits of virtual address, A12-A21, and output 10 bits of physical address, MA12-MA21. Bits MA12-MA19 are used to address onboard memory. This two-bit difference accounts for an 4 to 1 ratio of 4 MB virtual memory to 1MB physical memory.

The page map is composed of static RAM chips (21C, 22C, 19C, and 20C). The RAM chips are addressed by 10 bits from the system address bus (A12-A21). Note that the chips are always enabled on pin 8. The page RAM's output a 10-bit address (MA12-MA21), 5 status bits (PS0-PS4), and a write-enable bit (WE+).

Bits MA12-MA19 go directly to the memory address multiplexers (MUX's) and are considered physical address bits. MA21 is used to determine if memory is in base memory or on the memory expansion board. PS2, PS3, and PS4 are not used by the software as shipped, but are available for future memory management enhancements. PS0 and PS1 are used to provide the operating system with the following page status information:

PS0	PS1	Status of Page
0	0	Page not present
0	1	Present but not accessed
1	0	Accessed but not written
1	1	Written to (dirty)

Selecting RAM Row

Sheet 17 shows the RAM row decoder, 6J. RAM is divided into two rows of RAM chips, each row containing 512Kbytes. Address bit A1 is decoded to enable a particular row of RAM as follows:

LA1 Row Enabled

0	Row Y
1	Row Z

Address Multiplexing

The 64K dynamic RAM chips (see sheets 19 and 20) have 9 address inputs that are multiplexed to form the required 18-bit address. This is done through the row address strobe (RAS) and the column address strobe (CAS) inputs to pins 4 and 15 of these chips. Sheet 18 shows the memory address MUXs. Multiplex chips switch the RAM address input from row to column address. Notice there are two sets of MUXs, one set for each of the two rows of memory. Each set of MUXs outputs to one of the two buses: Y bus, or Z bus. These buses carry 9 bits of address directly to their respective row of memory. They first transfer 9 bits of RAS address and then 9 bits of CAS address.

As inputs, each set of MUXs receives MA12-MA9, A3-A11, and LA2. MA12-MA9 is the page address from the outputs of the page mapping RAMs. These bits address the selected physical page of memory. LA2, A3-A11 is the word address from the system bus. These bits are not altered by memory management. They address a word on the selected page. A3-A10 is gated through the MUXs at RAS time. A11 and MA12-MA18 are gated through at CAS time.

Table 2-4 Summary of Address Bit Assignments

Address Bit	Assignment
PA23	When = 0, fast bus cycle When = 1, slow bus cycle
PA22	When = 0, memory access When = 1, I/O access
A12-A21	Virtual page address to map RAMs
MA21	When = 0, base memory enabled When = 1, expansion memory enabled
MA20	Used to select expansion slots
MA12-MA19	Page address from page mapping RAMs
A3-A11	Word address from system address bus
A1-A2	Word address bits from system bus used to select a row of RAM chips
A0	Internal to 68010; always zero

Write Sequence: Processor to Page Map

A reference to the page mapping RAM is considered a CPU fast cycle, which is 400 ns or four cycles of the processor clock. When a time reference is made in the following text--for example, DTACK* is generated at 190 ns--it means 190 ns from the rising edge of the first PCLK in the cycle. Note the position of the asterisk in the following diagram:



Sheet 5--Asserting address and control signals:

- o At 60 ns into the fast cycle, the 68010 outputs the function code: FC2, FC1, or FC0. In this case, FC2 is high because the CPU has to be in supervisor mode to refer to the page map.
- o Also at 60 ns, the processor places the address on PA23-PA1. PA23 and PA22 will be 0 and 1, respectively, signifying a fast-cycle access to RAM.
- o At 120 ns the CPU outputs AS-, UDS-, and/or LDS-. The processor also asserts R/W* low at this point.
- o Gate 22D asserts PDS+.

Sheet 3--Starting memory timing:

- o PA23 applies a low to pin 9 of 16H; pin 8 of 16H is an inactive BGC+ (low). 16H outputs high to 19K; pin 3 of 19K is clocked. 19K clocks F/F 21E clear because of the inactive ROMLMAP* tied to its K input. This asserts ENRAS* (low) and starts delay line 19H.
- o ENRAS* is generated at 100 ns. Note that the signals generated from the delay line are time referenced to the generation of ENRAS*.

Logic Board Theory of Operation

Sheet 9:

- o ENRAS* (low) causes the DMA address IC to assert BGACK* for 200 ns. ENRAS* and R/W* assert FWR*.

The system address space allocated for the page mapping RAM includes addresses 400000-4007FF. These addresses are decoded to enable the page map.

PA23	PA22	PA21	PA20	PA19	PA18	PA17	PA16
0	1	0	0	0	0	0	0

Sheet 17:

- o Decoder 6J is enabled by ENRAS*. It is addressed by SPA23 and PA22, which are 0 and 1, respectively. This causes the decoder Q1 output to go low, thus asserting GATE1*.

Sheet 4--Enabling map RAM:

- o 1 of 8 decoder 26G is enabled by GATE1* (pin 5), PA19 = 0 (pin 6), the active SUPV+, and the inactive BGC* (pin 4). It is addressed by PA16-PA18, all equal to 0. The decoder drives pin 15 low, generating MRAMEN* (map RAM enable).
- o MRAMEN* goes to sheet 5, where it disables the processor data transceivers, and to sheet 16.

Sheet 16--Page map:

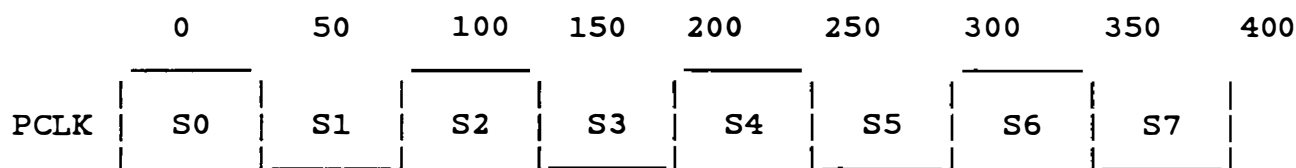
- o 19C, 20C, 21C, and 22C are the page-mapping RAM chips. They are 100 ns, 1K x 4, static RAM's.
- o The processor addresses the page map with address bits PA1-PA10 through buffer chips 16G and 12F. These chips are enabled by MRAMEN*.
- o The data is gated to the RAM chips via transceivers 23C and 24C.
- o The RAM is enabled for a write by gate 20E (pin 11).

Sheet 3--Acknowledging transfer by generating DTACK:

- o MUX 19F is set up to select the A inputs because we are not in expansion memory. At T90 pin 9 goes high, partially enabling 27F. An inactive BGC* and an inactive BMSEL* fully enable the gate. The high output from 27F (pin 8) generates DTACK* from 27N (pin 5) at 190 ns.
- o The processor samples DTACK* at 250 ns, verifies it at 300 ns, and latches the data at 350 ns.

68010 Local RAM Read Sequence

A reference to RAM is considered a CPU fast cycle, which lasts 400 ns or four cycles of the processor clock.



Sheet 5--Asserting address and control signals:

- o At 60 ns into the fast cycle, the 68010 outputs the function code: FC2, FC1, or FC0. The R/W* signal is negated (high) because data is being read.
- o Also at 60 ns, the processor places the address on PA23-1. PA23 and PA22 are 0, signifying a fast-cycle access to RAM.
- o Processor address buffers 16F and 17F are enabled by an inactive MRAMEN* and an inactive BGC* from gate 25N.
- o Transparent latch 17G is enabled on pin 1 by the inactive BGC+. It is put into transparent mode via 27H by an inactive MMUWREN+ and an inactive MMUWREND+.
- o At 120 ns, the CPU outputs AS-, UDS-, and/or LDS-.
- o Gate 22D generates PDS+.

Logic Board Theory of Operation

Sheet 3--Starting memory timing:

- o PA23 is low and feeds pin 9 of 16H; pin 8 of 16H is an inactive BGC+. 16H outputs high to 19K; pin 3 of 19K is clocked. 19K clocks F/F 21E clear because of the inactive ROMLMAP* tied to its K input. This generates ENRAS* and starts delay line 19H.
- o ENRAS* is generated at 100 ns. Note that the signals generated from the delay line are time referenced to the generation of ENRAS*.

Sheet 16--Obtaining physical address from page map:

- o The page mapping RAM's (19C, 20C, 21C, and 22C) are always enabled because of the ground on pin 8. Gate 26M sets them up for a read because of the inactive MRAMEN*.
- o The RAM's are addressed by virtual address bits A12-A21 and output physical address bits MA12-MA21 along with five page status bits.

Sheet 18--Driving the address to memory:

- o The address MUX's are always enabled by a ground on pin 15. The select input (pin 1) is high for the first 160 ns of the cycle and gate through the row address. After 160 ns, the column address is gated to memory.

Sheet 16--Strobing the row address:

- o Transparent latch 25F is in its transparent mode before T150 and passes address bits A1 and A2 through to become LA1 and LA2. At T150 pin 11 goes from high to low and 25F latches its data.

Sheet 17:

- o The RAM row decoder (6J) is enabled by a low PA22 via gate 20F. LA1 and LA2 select one of the four rows of RAM as shown in Table 2-5, the respective 4J gate and partially enables one of the 3J gates. At 130 ns, RAS goes out to the selected row of memory (T30*).

Table 2-5 Row Address Strobing

LA2	LA1	RAS Enabled	Row Affected
0	0	RAS0*	Row W
0	1	RAS1*	Row X
1	0	RAS2*	Row Y
1	1	RAS3*	Row Z

Sheet 2--Strobing the column address:

- o With PA22 low and BGC+ inactive, gate 26M outputs low to 22D, generating CASEN+.
- o MMU PAL 24G outputs only CASDIS* during a MMU error. This signal prevents a memory reference in the event of an error condition (such as a page fault).

Sheet 16:

- o The inactive CASDIS* and CASEN+ feed gate 24P, forcing a low onto pin 5 of 27H. Pin 6 is low for a read operation. 27H outputs high to 26M and 26M outputs high to 25F, generating ENCAS+.

Sheet 17:

- o ENCAS+ partially enables decoders 7J and 9J, LDS* and UDS* further enable the decoders, and at T90, one or both of the decoders are fully enabled. Note that LDS* and UDS* control byte or word selection.
- o The decoders are addressed by LA1, LA2, and LMA21. If LMA21 is low, LA1 and LA2 generate CAS to one of the rows of memory. If LMA21 is high, the target memory address is on the expansion board and no CAS goes to base memory.

Sheet 19--Accessing RAM:

- o At 130 ns into the bus cycle, RAS strobes in the row address. At 160 ns, the address MUX's switch from row address multiplexing to column address multiplexing. At 190 ns, CAS strobes in the column address.

Logic Board Theory of Operation

- o After access time (150 ns from RAS), the data is available on the RD bus.

Sheet 20--Putting information on the system data bus:

- o 12C and 12D are the RAM data transceivers. They are enabled during CAS time, provided address bit 21 is a 0 (base memory).
- o The direction in which the transceivers pass data is controlled by R/W* from the processor. For a read operation, they route the data from the RD bus to the D bus.

Sheet 3--Stopping memory timing and resetting ENRAS* via PDS+:

- o Gate 18G stops memory timing. Pin 13 is high when the bit map is not being referenced. Pin 12 is high when PDS+ is active. Pin 11 is high when no bus grant common is active, and pin 1 goes high at T120. These conditions cause 18G to output a low to gate 16H.
- o 16H outputs high to the D input of F/F 16K. At the next 1PCK+, MMUWREN+ is generated.
- o MMUWREN+ is tied to the D input of F/F 18H, and the trailing edge of the next PCK* sets the F/F.
- o 18H outputs low on pin 3 and sets the ENRAS F/F (21E).

Sheet 3--Acknowledging the transfer and generating DTACK*:

- o MUX 19F is set up to select the A inputs because we are not in expansion memory. At T90 pin 9 goes high, partially enabling 27F. An inactive BGC* and an inactive BMSEL* fully enable the gate. The high output from 27F generates DTACK* from 27N at 190 ns.
- o The processor samples DTACK* at 250 ns, verifies it at 300 ns, and latches the data at 350 ns.

Sheet 10--Checking parity:

- o The DMA data IC outputs UPARIN if bad parity (odd) is found in the high byte and LPARIN if a problem occurs in the low byte. Parity is checked during a read. During a write, LPARIN and UPARIN set the data into the memory parity chips so that the data byte plus the parity bit have odd parity.

Sheet 17:

- o Gate 13H outputs low at CAS time when a read to base memory is being done. This output, along with the data strobes, enables one or both of the gates feeding 12H.
- o 12H outputs low when there has been a parity error. When T90 goes from low to high, F/F 6K resets and 20E presents PERR* to the system.

Sheet 6:

- o PERR* forces a low out of 28F. If the error enable bit is active, a low is gated to pin 4 of 18F. Decoder 18F presents a level 7 interrupt to the processor.

Parity

Figure 2-2 is a simplified schematic of the parity generator circuit in the custom gate array simulator board.

Parity Write

During a RAM write operation the parity circuit determines if the number of bits set to a one in the upper or lower data byte is odd or even. If the number is even the parity bit for that byte is set hi. If the number is odd, the parity bit is set low. Parity is checked during a 68010 RAM read cycle. If parity is incorrect a level seven interrupt is generated. The ENCAS* input to the parity error generating circuit on sheet 17 prevents generation of a parity error during a page fault. The LDS input prevents parity error during a DMA RAM memory access.

Sheet 17:

- o During a write, the BP+ bit is low and the select input S to the multiplexer 10J is high; thus UMUXPAR and LMUXPAR are both hi during a write.

Logic Board Theory of Operation

The odd-parity generators in the DMA data gate array (sheet 10) generate the odd parity signals UPARIN (upper-byte parity) and LPARIN (lower-byte parity). If the data on the data bus has an even number of high bits, the hi input from UMUXPAR makes the number of high inputs to the 74LS280 odd, and the parity bit input to RAM is hi. If the number of highs on the data bus is odd, then adding the hi input from UMUXPAR or LMUXPAR keeps the total input to 74LS280 even and the output of the DMA data away is low. Thus the two combined inputs to RAM, D0-D7 plus LPARIN and D8-D15 plus UPARIN, always have odd parity.

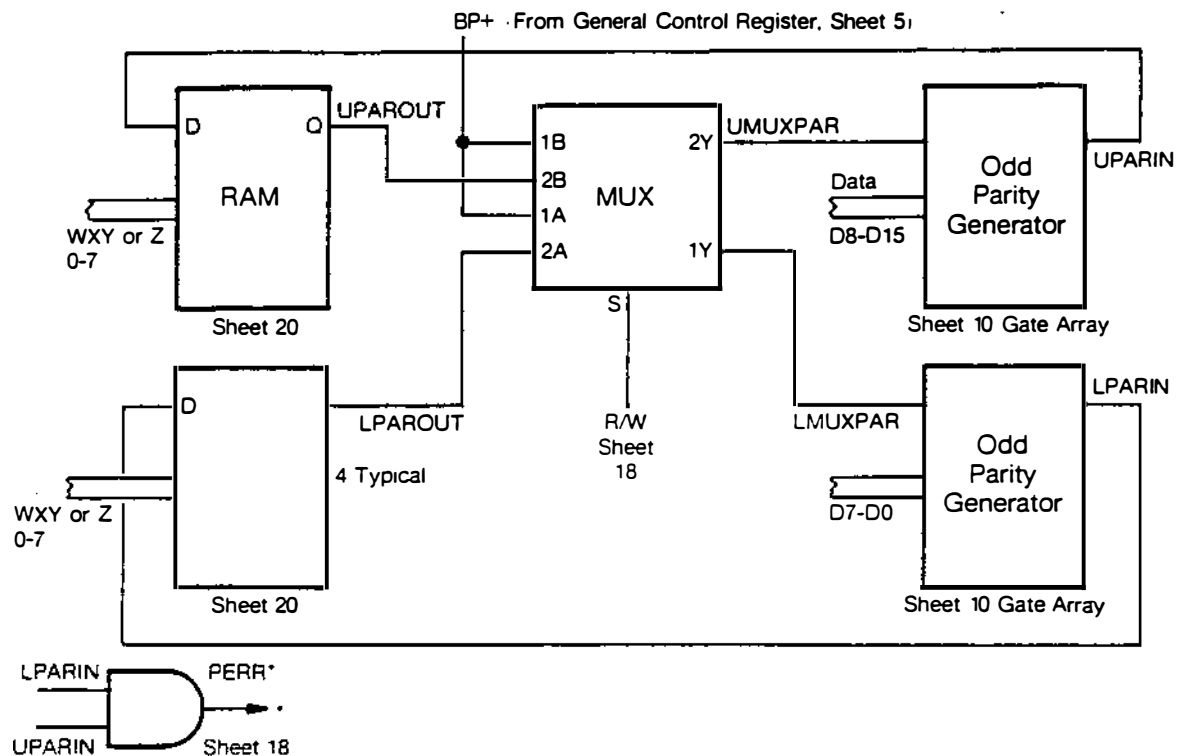


Figure 2-2 Parity Generator

Parity Check

During a memory-read operation, the two parity generator chips check the parity of the 8-bit bytes plus their corresponding parity bit. Thus, during a RAM read, both UPARIN and LPARIN should be low, indicating even parity. If either signal is high, circuitry on sheet 18 generates a parity error (PERR*). The PERR* signal is used by the 68010 interrupt logic on sheet 6. An interrupt is generated if the parity error-enable is asserted at the general control register (GCR). The PERR* signal latches the current bus status into the bus status register (BSR) and the general status register (GSR). If the supervisor program has not masked out the error with the error enable bit at the GCR, the PERR* generates a level 7 interrupt.

Page Status Update and Memory Management Errors

Each memory access to RAM is checked for validity. If it is a valid access, the status bits in the map RAM's are updated. If it is not valid, the attempted access to memory must be prevented and an error signal must be generated. The circuitry to accomplish this is explained below.

The memory management unit write (MMUWR*) signal originates on sheet 2. On sheet 16, it updates the status of the page status registers. This signal is asserted each time an access to RAM is made that does not produce an access error. On sheet 2 MMUWR* enables tristate buffers that load the new page status bits PS0 (page status bit zero), PS1, and WE (write enable). On sheet 16 MMUWR* puts the map status RAMs into a write condition so that the new status of PS0, PS1, and WE is written into the RAM's during each valid RAM access.

On sheet 2 MMUWR* is asserted by MMUWREN+ (memory management enable) high and MMUERR* (memory management unit error) high, no error, and CASEN+ (column address strobe enable).

MMUWREN+ is enabled each time an access to RAM is made by the 68010 or the DMA interface unit.

The memory management PAL generates the following new page status:

- o PS1: Set to 1 regardless of previous state to indicate a read has taken place.
- o PS0: Set to 0 during a memory read if there is no memory error. Otherwise, it is set to 1.
- o WE+: Set equal to SPA23. Pages are write enabled when and only when they are accessed in supervisory mode by the 68010.

Generation of Memory Management Interrupts

If the EE+ bit is set high on sheet 6, the MMUERR* generates a level 7 interrupt. The memory management PAL generates two signals that drive the interrupt logic on sheet 6: PGF (page fault) and MMUERR (memory management unit error).

Logic Board Theory of Operation

Page Fault

This signal is asserted whenever both PS0 and PS1 are 0 and the 68010 is executing a user program, FC2 is low, or a DMA RAM access (BGC+ asserted) is taking place. When PS0 and PS1 are both 0 a page fault is not generated when the 68010 accesses the page in supervisory mode.

Memory Management Error

The three ways to generate a memory management error are:

- o Page fault
- o User attempt to access the kernel, indicated by:
Kernel access--A19, A20, and A21 all low
User program execution--PA22, SUPV, and BGC all low
- o User access to a page that is not write enabled, indicated by:
Page not enabled for a write--LWE low
User program execution--PA22, SUPV, and BGC all low

Bus Error

The memory management unit also has an output called BERR (bus error). This signal goes directly to the 68010 on sheet 4. It is caused by the following conditions:

- o CPU page fault: page not present
- o User I/O fault (access to address not in RAM)
- o User attempt to write to a page that is not write enabled
- o User attempt to write to the kernel.

Column Address Strobe Disable

The column strobe disable (CASDIS) signal is generated by the memory management PAL to prevent the completion of an illegal access to RAM.

Refresh Operation

Circuitry for refresh is contained in the DMA address gate array shown on sheet 9. The 42S6 dynamic RAM chips in physical memory (sheets 19-22) must be refreshed at least every 4 ms to prevent data loss. A RAS only refresh is used--that is, 256 row addresses are strobed to all rows of RAM every 4 ms. This means that 64 refresh cycles must be accomplished every millisecond.

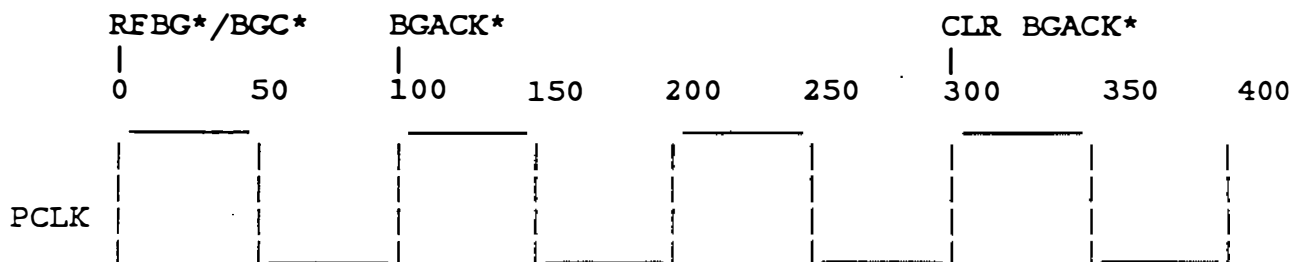
Two 8-bit counters in the DMA address IC constitute most of the refresh circuitry. One is used as an address counter and the other is used to time the refresh requests.

The request counter is clocked by 1PCK+. It presents RFRQ* to the bus arbitration circuitry on every 144th 1PCK+. In other words, it is configured as a divide by 144 circuit.

The address counter is incremented by the refresh bus grant (RFBG*). It drives row addresses onto the system bus. This counter cycles through the 256 row addresses (0-FF), driving a different address onto the system bus for each refresh bus grant.

Sheet 9--Getting bus control and driving address:

- o The DMA address IC asserts RFRQ* on every 144th occurrence of 1PCK+.
- o When the RFRQ* has priority, the arbiter PAL grants the refresh circuitry control of the system bus by returning RFBG* and BGC* (bus grant common).
- o The DMA address IC acknowledges receipt of the bus grant by asserting BGACK*, which causes the bus arbiter to latch RFBG* and BGC*.
- o BGACK* also determines how long mastery of the bus lasts by latching the grants. BGACK* remains active for two clock cycles during a refresh.



Logic Board Theory of Operation

- o The refresh circuitry internal to the DMA address IC then drives the 8-bit refresh address onto the system bus (A3-A10).

Sheet 3--Starting memory timing:

- o F/F 18H (pin 6) is set when the system is idle, because BGC+ and ENRAS+ are absent. F/F is used to start memory timing for bus masters other than the CPU.
- o When bus control is granted to the refresh circuitry by the bus arbiter, the common bus grant is generated (BGC+).
- o This causes F/F 18H to reset, 19K clocks F/F 21E clear, and memory timing is started.

Sheet 17--Refreshing RAS:

- o RFBG* enables all of the 4J gates to output lows, partially enabling the 3J gates. T30* fully enables the 3J gates, asserting RAS to all rows of memory.

Sheet 2:

CASEN+ is not generated because gate 26M is broken by BGC+, and gate 22D is broken by an inactive NRE/BGC*.

System Control and Status Registers

Various control and status registers are available to the processor. These registers monitor system status and control the hardware. Tables 2-6 through 2-11 describe these various registers.

Table 2-6 General Status Register--Address 410000 (Read Only)

Data Bit	Signal	Description
14	R/W-	0 = Write cycle, 1 = Read Cycle
13	NPC+	1 = Nonprocessor cycle
12	PF-	0 = Page fault; applies to the processor (supervisor or user) and the DMA controller
10	PIE+	1 = Parity interrupts enabled
08	UIE-	0 = User access to memory above 4 MB

Information in the general status register is updated with each bus cycle. If the current cycle causes a parity error, MMU error, or processor bus error, the information in the GSR is not updated at the following cycles until the clear status register signal is received. This signal is generated when the processor writes to address 4C0000.

The general status register is on sheet 6 (24D) of the schematics.

Table 2-7 Bus Status Register 0--Address 430000 (Read Only)

Data Bit	Signal	Description
15	MMUERR-	0 = MMU error; three possible causes: (1) Processor or DMA page fault (2) User write to write protected page (3) User access to kernel (0-512K)
14	DKBG-	0 = Disk DMA cycle
13	EXP0BG-	0 = Expansion board 0 DMA cycle
12	EXP1BG-	0 = Expansion board 1 DMA cycle
11	EXP2BG-	0 = Expansion board 2 DMA cycle
10	EXP3BG-	0 = Expansion board 3 DMA cycle
09	UDS-	0 = Upper byte access
08	LDS-	0 = Lower byte access
07	PA23	Processor address bit 23
06	PA22	Processor address bit 22
00-05	A16-A21	Logical address bits 16-21

Note

The bus status register is on sheet 6 of the schematics.

Table 2-8 Bus Status Register 1--Address 440000 (Read Only)

Data Bit	Signal	Description
00-15	A00-A15	Latches address during NMI or BERR

Note

The bus status registers (BSR0, BSR1), located on sheet 6 in the schematics, are composed of transparent latches: 18C and 25D are BSR0; 16B and 21D are BSR1. They latch information pertaining to the status of the bus when there has been a bus, parity, or MMU error. They can be useful when troubleshooting hardware problems or debugging code. The BSRs are not cleared by reset; therefore, they can be read easily from the debugger.

Table 2-9 General Control Register--Address E4X000 (Write Only)

Address	Bit Signal	Description
E40000	15 EE+	1 = Error enable 0 = Error disable, meaning no level 7 interrupt or bus error can occur
E41000	15 PIE+	1 = Parity error circuit and interrupt are enabled 0 = Parity is disabled
E42000	15 BP+	1 = Memory write cycle resulted with parity error 0 = Memory write cycle resulted with good parity
E43000	15 ROMLMAP	0 = Processor is forced into ROM address space 1 = Normal addressing
E44000	15 L1 MODEM*	0 = Modem connected to line 1
E45000	15 L2 MODEM*	0 = Modem connected to line 2
E46000	15 D/N CONNECT*	0 = Dial network connected to line 1

Note

The general control register is located on sheet 6 of the schematics. It is an addressable latch (7K). The processor addresses the GCR with address bits A12, A13, and A14. The various control signals are enabled and disabled using processor data bit 15.

**Table 2-10 Miscellaneous Control Register--Address 4A0000
(Write Only)**

Data Bit	Signal	Description
15	CLRSINT-	Dismisses the level 6, 60-Hz interrupt. To dismiss the interrupt, the bit must be toggled from high to low and back to high. When this bit is low, it makes the interrupt.
14	DMAR/W-	0 = Disk DMA write operation 1 = Disk DMA read operation. This bit, along with the IDMAR/W- bit in the disk DMA count register, should be updated before a disk DMA operation.
13	LPSTR+	Strobes data from the line printer data register to the line printer through Centronics interface protocol. After data is set up at the data register, LPSTB+ must be toggled from low to high and back to low to strobe the data to the printer.
12	MCKSEL-	0 = Modem RX clock and TX clock gated to the communication controller's RX clock and TX clock inputs 1 = Programmable timer selected to generate the clock pulses for the communication controller.
11	LED3-	0 = Red LED 3 (CR21) on 1 = Off
10	LED2-	0 = Green LED 2 (CR22) on 1 = Off

Table 2-10 Miscellaneous Control Register -- Address 4A0000
(Write Only) (Continued)

Data Bit	Signal	Description
09	LED1-	0 = Yellow LED 1 (CR23) on 1 = Off
08	LED0-	0 = Red LED 0 (CR24) on 1 = Off

Note

The miscellaneous control register is located on sheet 15 of the schematics.

Reading General Status Register (Address 410000)

The processor accesses the system status and control registers by performing a fast bus cycle. This operation is similar to the previous fast cycles discussed. The processor drives address and control signals and waits for DTACK*. The address decode is the only difference between this and previous fast cycles.

PA23	PA22	PA21	PA20	PA19	PA18	PA17	PA16
0	1	0	0	0	0	0	1

Sheet 4--Decoding address:

- o GATE1* is active for all fast cycles other than accesses to main memory. This signal enables decoder 26G on pin 5.
- o The processor must be in supervisor mode to access the GSR, and BGC* is not active during process bus cycles. These conditions cause gate 25N to enable the decoder on pin 4.
- o When addressing the GSR, PA19 = 0, which fully enables the decoder (pin 6).
- o The decoder is addressed by PA18, PA17, and PA16. As the chart above illustrates, these bits are 0, 0, and 1, respectively. This causes the decoder to generate GSRRD* from pin 14.

Sheet 6--Driving the data:

- o The general status register is transparent latch 24D. Its outputs are enabled by GSRRD*, and it Sheet 3--Acknowledging data transfer:
- o Gate 27F causes the generation of DTACK* at T90. The processor latches the data on the trailing edge of the third PCK+, the DMA address array.

Interrupting the Processor

Interrupts inform the processor of special situations within the system. They interrupt normal processing and cause the CPU to be vectored into a routine to deal with the special situation. Motorola calls this exception processing.

The processor can mask interrupts by manipulating bits 12, 11, and 10 of the 68010's status register. For example, if these bits are loaded with a binary 100, interrupt priority levels (IPL) of 4 and below are ignored. IPL7 interrupts cannot be masked; this is the nonmaskable interrupt (NMI). If bits 12, 11, and 10 are all set to 1's, all interrupts except the level 7 interrupt are masked.

Exception processing is the only way to go from the user state to the supervisor state. It occurs in these four steps:

- o A temporary copy of the status register is made and the status register is set for exception processing (all interrupts equal to the current level and below are masked and the S bit is set, which puts the processor into the supervisor state).
- o The exception vector is determined.
- o The current processor context is saved (status register and program counter are pushed onto the supervisor stack).
- o New context is obtained and instruction processing resumed.

Exception Vectors

Exception vectors are memory locations from which the processor fetches the address of a routine to handle an exception. Exception vectors are words in length, and all exception vectors lie in supervisor data space. Exception vectors are obtained through the use of a vector number, which is an 8-bit value that, when multiplied by 4, gives the offset of the exception vector. The 68010 can accept an externally generated vector number or generate the vector number internally.

As implemented in the UNIX PC, all vector numbers are generated internally by the 68010 microcode. This is called auto-vectoring. Once a vector has been calculated, the processor fetches an address from that location in memory. The processor loads the address into the program counter and begins executing instructions. Typically, it is then vectored into the interrupt service routine.

Table 2-11 shows the interrupt vector number generated for each interrupt and the hexadecimal offset calculated from each vector number. If a level 2 interrupt is received, the 68010 generates a vector number of 26. It then reads two words beginning at address 68H, loads the words into its program counter, and begins executing instructions.

Table 2-11 Interrupt Vector Numbers and Hexadecimal Offsets

Vector Number (Decimal)	Offset (Hex)	Assignment
25	64	Level 1 interrupt autovector
26	68	Level 2 interrupt autovector
27	6C	Level 3 interrupt autovector
28	70	Level 4 interrupt autovector
29	74	Level 5 interrupt autovector
30	78	Level 6 interrupt autovector
31	7C	Level 7 interrupt autovector

Logic Board Theory of Operation

The interrupt logic is located on sheet 6 of the schematics. Seven levels of interrupts are implemented through the use of three interrupt priority level signals (IPL0, IPL1, and IPL2). IPL7, the NMI, is the highest priority interrupt. It cannot be masked by software. IPL1 is the lowest priority interrupt. An interrupt priority level of 0 means no interrupts are pending. The following table lists the interrupts and their priority levels:

Table 2-12 Interrupts and Their Priority Levels

IPL	Interrupt
7	Nonmaskable interrupt
6	Realtime interrupt
5	Interrupt from expansion board 1 or 2
4	RS-232 interrupt
3	Keyboard interrupt
2	Floppy/hard disk/line printer interrupt
1	Interrupt from expansion board 3 or 4
0	No interrupts

Interrupts: Theory of Operation

The interrupts operation is as follows:

Sheet 6:

- o The various interrupts are active low inputs to encoder 18F. Pin 4 is the NMI, the highest priority interrupt. If this interrupt is active, the encoder drives IPL0, IPL1, and IPL2 all high. This presents a binary encoded IPL7 interrupt to the processor.
- o Because pin 10 of the encoder is grounded and if no interrupts are present, the encoder drives IPL0, IPL1, and IPL2 low. This informs the processor that no interrupts are present. The IPL signals input directly to the processor.

Sheet 5:

- o If any of the IPL inputs to the processor are low, the 68010 detects an interrupt. The processor then acknowledges the interrupt and begins exception processing.

- o When the 68010 acknowledges an interrupt, it drives FC0, FC1, and FC2 high. Address bits A4-A23 are also driven high. Address bits A1-A3 encode the level of interrupt being acknowledged.
- o Gate 13H generates a signal called INTA*, which goes to sheet 3 and prevents an I/O request from being generated.
- o 13H also partially enables 13E. When PAS* is asserted, 13E generates VPA* (valid peripheral address). During an interrupt acknowledge, this signal replaces DTACK* and handshakes the processor. It also tells the processor that the interrupt being acknowledged is an autovector interrupt. Since this signal is generated with every interrupt being acknowledged, all interrupts are autovectored.

Note

Acknowledging the interrupting peripheral is the responsibility of the software. Typically, this is handled in the interrupt service routine.

Disk Direct Memory Access (DMA)

This section explains logic board circuitry that transfers information between a disk drive and RAM memory.

Disk Format and Flow

Data from a disk drive passes through three sections of hardware before it reaches RAM memory:

- o Serial data from the disk drive, consisting of both data and clock pulses, is separated into a clock signal and a data signal. For the hard disk, this is done by the data separation circuitry shown on sheet 12 of the schematics. For the floppy disk, it is done by the WD2797 floppy disk controller.
- o Serial data is assembled into 8-bit bytes by the disk controller. The disk controller for the hard disk is the WD1010; for the floppy disk, it is the WD2797.
- o The disk DMA bus interface assembles 8-bit bytes into 16-bit words and writes them into a RAM memory location. The RAM address is contained in the bus interface.

Logic Board Theory of Operation

Disk Program Summary

Data on disk is located by three parameters: cylinder, head, and sector. The disk DMA bus interface has two parameters: DMA starting address and word count. These parameters plus the disk commands are written in the following disk program sequence summary:

- o System register disk bits are set. These bits select the disk drive and head number; in the case of the floppy disk, they turn on the motor.

Counters in the DMA disk bus interface are loaded with the starting address and number of words to be transferred. The disk controller registers are loaded with the track and sector to read.

- o The 68010 starts the transfer of data from disk by writing a Read Sector command to the disk controller.
- o The disk DMA bus interface takes control of the bus through bus arbitration and transfers data from the disk controller into RAM memory. Data passes through the three sections of hardware as described above. One disk DMA bus interface unit is shared by both the floppy and hard disk controllers.

When the sector of a disk is being read, the disk DMA bus interface reads two 8-bit bytes from either the WD1010 hard disk controller or the WD2797 floppy disk controller, assembles them into one 16-bit word, and writes the word into RAM memory.

When data is being transferred from RAM memory to disk, the disk DMA bus interface reads a 16-bit word from RAM memory, separates it into two 8-bit bytes, and loads them into the data register of either the WD1010 hard disk controller or the WD2797 floppy disk controller.

The disk DMA bus interface consists of two custom gate array chips: the DMA address IC shown on sheet 9 and the DMA data IC shown on sheet 10. Once a Read Sector command is written to the disk controller command register, the disk DMA bus interface takes control of the bus through bus arbitration each time a word is to be transferred to memory. Between word transfers, the 68010 can access the bus. The software must be written so that the 68010 does not write to the disk controllers while a command is in progress.

- o The disk controller informs the 68010 when it has completed a command by asserting its interrupt output.

Definitions

Disk Commands

Disk commands control the movement of data to and from memory to the disk storage medium. The disk commands are described below.

DMA read and DMA write are defined with respect to the disk DMA bus interface that is the bus master during the transfer. During a DMA read, data is moved from RAM to the word buffer in the bus interface. During a DMA write, data from the word buffer in the disk DMA bus interface is written to RAM.

The disk controller Write Sector and Read Sector commands are defined with respect to the controller. A Read Sector command moves data from the disk to the disk controller. A Write Sector command moves data from the controller to the disk, and the controller writes to disk.

Thus, to move data from RAM to disk requires a DMA read and a disk Write Sector command. To move data from disk to RAM requires a disk Read Sector command and a DMA write transfer.

Logic Board Theory of Operation

System Register Disk Bits

Disk operation is selected by writing instruction to the disk control register as explained below.

Disk Control Register (Drive and Head Select), Table 2-13.

Before a disk operation can occur, the drive and head must be selected. The processor does this by writing to address 4E0000, the disk control register (sheet 11).

Table 2-13 Disk Control Register--Address 4E0000 (Write Only)

Data Bit	Signal	Description
07	FDRST-	0 = Floppy disk controller reset 1 = Not reset
06	FDR0+	0 = Floppy drive 0--not selected 1 = Floppy drive 0--selected
05	FDMTR+	0 = Floppy drive motor is not on 1 = Floppy drive motor is on
04	HDRST-	0 = Hard disk controller reset 1 = Not reset
03	HDR0+	0 = Hard disk drive 0--not selected 1 = Hard disk drive 0--selected
00-02	HDHSEL 0-2	These three bits are decoded to select the head

Miscellaneous Control Register (DMA Read/Write), Table 2-14.

This register controls the DMAR/W- bit used by the disk PAL shown on sheet 2 and other bits shown in the following table:

**Table 2-14 Miscellaneous Control Register--Address 4A0000
(Write Only)**

Data Bit	Signal	Description
15	CLRSINT-	This bit dismisses the level 6, 60-Hz interrupt. To dismiss the interrupt, the bit must be toggled from high to low and back to high. When this bit is low, it masks the interrupt.
14	DMAR/W-	0 = Disk DMA write operation 1 = Disk DMA read operation. This bit, along with the IDMAR/W-bit in the disk DMA count register, should be updated before a disk DMA operation.
13	LPSTR+	This bit strobes data from the line printer data register to the line printer through Centronics interface protocol. After data is set up at the data register, LPSTB+ must be toggled from low to high and back to low to strobe the data to the printer.
12	MCKSEL-	0 = Modem RX clock and TX clock are gated to the communication controller's RX clock and TX clock inputs. 1 = Programmable timer is selected to generate the clock pulses for the communication controller.
11	LED3-	0 = Red LED 3 (CR21) on; 1 = off
10	LED2-	0 = Green LED 2 (CR22) on; 1 = off
09	LED1-	0 = Yellow LED 1 (CR23) on; 1 = off
08	LED0-	0 = Red LED 0 (CR24) on; 1 = off

Logic Board Theory of Operation

Line Printer Status Register (Controller Interrupt), Table 2-15

Bits D2 and D3 of this register are set high when the disk controller completes a command. These bits may be polled by the 68010. They are reset when the status register of the controller is read.

**Table 2-15 Line Printer Status Register--Address 4A0000
(Write Only)**

Data Bit	Signal	Description
07	LPBUSY+	1 = Line printer is busy
06	LPSELECT+	1 = Line printer is selected
05	LPNOPAPER+	1 = Line printer has no paper
04	ERROR*	0 = Line printer error condition
03	FDINTRQ+	1 = Floppy disk controller interrupt
02	HDINTRQ+	1 = Hard disk controller interrupt
01	PERR*	0 = Main memory parity error has been detected; this bit can be cleared with the CSR command (write to 4C0000)
00	DTDET*	0 = Dial tone is detected
15	CLRSINT-	This bit dismisses the level 6, 60-Hz interrupt

Hard Disk Controller (WD1010)

Hard disk control is provided by the Western Digital WD1010 Winchester disk controller chip. It provides MFM-encoded data and all of the control lines required by disks using the Seagate Technology ST506 or Shugart SA1000 interface standard. The WD1010 can provide control for two hard disk units.

Pin Functions (sheet 11) for the WD1010 are listed in Table 2-16.

Table 2-16 Pin Functions WD1010

Pin(s)	Signal Description
12-19:	Winchester data bits 0-7; used during programming and while transferring data to and from the drive.
9-11:	Address bits 0-2; used by 68010 while programming and reading the chip's various registers.
1:	Buffer chip select; asserted by WD1010 to enable the reading of or writing to the RAM data buffer.
8:	Chip select; enabled by 68010 when reading of or writing to a WD1010 register is desired. When CS is low, pins 6 and 7 are used as inputs.
7:	Write enable; when used as an input, it enables the bus master to write into the controller's internal registers. When used as an output, it allows the controller to write to the RAM buffer.
6:	Read enable; when used as an input, it allows the bus master to read the controller's internal registers. As an output, it allows the controller to read from the data buffer.
31:	Track 000; asserted by selected drive when heads are located over track 0.
32:	Seek complete; asserted by selected drive when heads are settled over selected track.

Table 2-16 Pin Functions WD1010 (Continued)

Pins	Signal Description
28:	Drive ready; asserted by selected drive to signal its capability to do reads, writes, and seeks. When signal goes low, all commands are deactivated.
30:	Write fault; asserted by selected drive if a fault is detected. When low, all commands are deactivated.
29:	Index; pulsed when index mark is detected. Indicates beginning of track.
35:	Buffer ready; normally used by data buffer to signal to the controller that it is ready to be read (full) or written to (empty). As implemented in the UNIX PC, this input is tied to a 0.6144-MHz clock that constantly tells the controller that the buffer is accessible.
3:	Interrupt request; generated by WDC upon termination of a command; cleared when status register is read.
5:	System reset.
27:	Step; 8.4-us pulses to drive stepping motor.
26:	Direction; when high, the heads move inward toward higher cylinder numbers. When low, the opposite is true.
23:	Early; output used to derive delay value for write precompensation. Valid when write gate is active.
22:	Late; output used to derive delay value for write precompensation. Valid when write gate is active.
33:	Reduced write current; goes high for all cylinder numbers greater than the value programmed into the write precompensation register.

Table 2-16 Pin Functions WD1010 (Continued)

Pins	Signal Description
24:	Write gate; an active high when write data is valid; used by drive to enable write current to data heads.
37:	Read data; MFM data pulses from disk.
25:	Write clock; 5-MHz clock used to derive write data rate.
34:	Data run; looks for a string of 0s in the read data, indicating the beginning of an ID field. If the 0s are detected, read gate (RG) is brought high.
38:	Read gate; set high for data and ID fields.
21:	Write data; open drain output that shifts out MFM data at the speed determined by the write clock input.
39:	Read clock; square-wave clock input derived from external data recovery circuits.

Task File Registers

The WD1010 is similar to the other LSIs that have been discussed in that it must be programmed before hard disk operations. The 68010 is required to supply information--such as drive, head, sector, number of sectors to transfer, and so on--to the task file registers before writing a command to the command register.

Table 2-17 Task File Registers

Address	Function
Data register (E00000)	Used during reads and writes to hold one byte of data
Error register (E00002)	Read by 68010 to determine what type of error occurred during a disk operation
Sector count register (E00004)	Data bits 0-7 are used during reads and writes to indicate the number of sectors to transfer
Sector number register (E00006)	Data bits 0-7 are used during reads and writes to indicate the sector address
Cylinder number low register (E00008)	Data bits 0-7 are used during reads and writes to indicate the current cylinder number
Cylinder number high register (E0000A)	Holds the upper byte of the current cylinder address
Sector drive head register (E0000C)	Bits 0-2, head number; bits 5-6 will be 0 and 1 indicating 512-byte sector; bit 7 is set for ECC and reset for CRC
Status register (E0000E)	Read by 68010 to determine current status of hard disk control circuits and data buffer
Command register (E0000E)	Written into by the 68010 to control step rate and issue disk commands

Error Register--E00002 (Read Only)

- Bit 7: Bad block detect used for bad sector mapping.
- Bit 6: CRC error.
- Bit 5: Forced to 0.
- Bit 4: ID not found. This bit is set to indicate that the correct cylinder, head, sector number, or size parameter could not be found or that a CRC error occurred on the ID field. This bit is set on the first failure and remains set even if the error is recovered on a retry. When recovery is unsuccessful, the error status bit is set also.
- Bit 3: Forced to 0.
- Bit 2: Aborted command. This bit is set if command is issued while the DRDY is deasserted or the WF is asserted. The aborted command bit is also set if an undefined command code is written into the command register.
- Bit 1: Track 0 error. This bit is set only by the Restore command. It indicates that TK000 has not gone active after the issuance of 1K of stepping pulses.
- Bit 0: Data address mark not found. This bit is set during a Read Sector command if the data address mark is not found after the proper sector ID is read.

Status Register--E0000E (Read Only)

- Bit 7: Busy. This bit is set whenever the WD1010 is accessing the disk. Commands should not be loaded into the command register while the busy is set.
- Bit 6: Ready.
- Bit 5: Write fault.
- Bit 4: Seek complete.
- Bit 3: Data request.
- Bit 2: Always 0.

Logic Board Theory of Operation

Bit 1: Command in progress.

Bit 0: Error. This bit indicates that a nonrecoverable error has occurred. If bit 0 is high, read the error register (E00002) to determine the type of error written into the control register.

Commands

The six commands that can be issued to the WD1010 are described in the following table:

Table 2-18 WD1010 Commands

Command	Function
Restore	Returns heads to track 0
Seek	Moves heads to cylinder in cylinder number register
Read Sector	Reads the contents of a sector
Write Sector	Writes data to a sector
Scan ID	Updates head, sector, and cylinder registers
Write Format	Formats one track

If the track selected in the cylinder registers is not the same as the track that the heads are currently positioned over, and a read or write command is issued, the controller executes an implied seek.

Typically, the WD1010 can be commanded to seek a track and then write to a sector. It is important to remember that the controller has to do a read before it can write. The reason for the read is that the controller has to locate the requested sector before it can write information to that sector. The WD1010 does this by reading the ID fields. Once it locates the target sector, the controller reads the first byte from the data buffer, converts the parallel data to MFM data, and transfers this MFM data to the disk.

Disk DMA Bus Interface Registers

Address Register--4DXXXX

When the DMA address counter is loaded, the four least significant digits of the address bus contain the DMA address. The DMA address counter contains two sections: one to hold the two least significant hexadecimal digits of DMA address and one to hold the four most significant digits of DMA address.

To load the counter requires two write cycles. A14 selects the section to be loaded. When A14 is low, the least significant DMA address counter is selected, see Table 2-19. In this counter, A1-A8 of the address bus correspond to A1-A8 of DMA address. When A14 is high, the most significant DMA counter is selected. In this counter, A1-A13 of the address bus correspond to A9-A21 of DMA address.

Thus the maximum DMA address that can be loaded is 3FFFFFF. This address is loaded in two writes as listed in the following table (note that the contents of the data bus are not used):

Table 2-19 DMA Address Count Register Selection

Address	Data	Description
4D00FF	xxxx	A14 is low; two least significant digits loaded
4D7FFF	xxxx	A14 is high; four most significant digits loaded

The counter is read and incremented when DKBG is asserted during execution of a Read/Write Sector command.

Count Register

The DMA count register is contained in the DMA data IC shown on sheet 10. The bit definitions for this counter are shown in Table 2-20.

The DMA count is incremented after each DMA transfer. When the count reaches 3FFFx, DMA operation is terminated; thus, the maximum number of words to be transferred for a single DMA operation is 16K words. The content of this register should not be modified during a DMA operation unless DMA abortion is desired by deassertion DMAEN+.

Table 2-20 Disk DMA Count Register--Address 460000

Data Bit	Signal	Write Description
15	DMAEN+	1 = Disk DMA enable 0 = Disable Reset clears this bit
14	IDMAR/W-	1 = Disk DMA read operation 0 = Disk DMA write operation
00-13	DC00-DC13	These bits represent the current transfer count
Data Bit	Signal	Read Description
15	U/OERR-	0 = Disk DMA underrun or overrun
00-13	DC00-DC13	These bits represent the current transfer count

Initializing Hard Disk DMA Read

This section lists the signal conditions necessary to initialize system register disk bits and the disk DMA bus interface and to load the WD1010 task file.

Loading Miscellaneous Control Register

The DMA R/W* bit is set by the miscellaneous control register, shown on sheet 15. It is enabled by a signal called MREG WR*, which is asserted by signals shown on sheet 4. The signal conditions that enable MREG WR* are listed in Table 2-21.

Table 2-21 Signal Status to Assert MREG WR*

Sheet	Signal	Status
4	A16	0
4	A17	1
4	A18	0
4	A19	1
4	FWR*	0
4	BGC*	1
4	SUP+	1
4	GATE1*	0
17	PA22	1
17	SPA23	0
17	ENRAS*	0

Logic Board Theory of Operation

Loading Disk Control Register

The disk drive and head-select bits are set by the disk control register, shown on sheet 11. It is enabled by HDCTLWR*, which is asserted by signals shown on sheet 4. The signal conditions that enable HDCTLWR* are listed in Table 2-22.

Table 2-22 Signal Status to Assert HDCTLWR*

Sheet	Signal	Status
4	A16	0
4	A17	1
4	A18	1
4	A19	1
4	FWR*	0
4	BGC*	1
4	SUP+	1
4	GATE1*	0
17	PA22	1
17	SPA23	0
17	ENRAS*	0

Loading DMA Address Counter

The status of address bits PA16-PA23 during the loading of the address counters is:

PA23	PA22	PA21	PA20	PA19	PA18	PA17	PA16
0	1	0	0	1	1	0	1

Listed below are the signal transitions to assert the DADD WR* signal, which enables the DMA address counter:

- o On sheet 3, PA23 low and BGC+ inactive cause F/F 21E to clock, generating ENRAS*.
- o On sheet 17, ENRAS* enables one of four decoder 6J. SPA23 and PA22 are equal to 0 and 1, respectively, causing the decoder to assert GATE1*.
- o On sheet 9, the DMA address IC asserts FWR* for fast-cycle writes (refer to sheet 5 of 6 in the UNIX PC gate array schematics).
- o On sheet 4, gate 25N is enabled because the 68010 is in supervisor mode and BGC* is high. This partially enables gate 26F by putting a low at 26F pin 5.
- o GATE1* fully enables 26F, which outputs a low to pin 4 of decoder 28G.
- o FWR* enables pin 5 of 28G.
- o PA19 is high and fully enables the decoder.
- o The select inputs of the decoder are tied to address bits A16, A17, and A18, which are 1, 0, and 1, respectively. This causes the decoder to drive pin 10 low, generating DADD WR*.

DADD WR* inputs to the DMA address IC (refer to sheet 5 of 6 in the UNIX PC gate array schematics).

Loading DMA Count Register

The DMA count register, located at address 460000, is loaded when DCNTCS* is asserted. The signal status that asserts DCNTCS* is shown in Table 2-23.

Table 2-23 Signal Status to Assert DCNTCS*

Sheet	Signal	Status
4	A18	High
4	A17	High
4	A16	Low
4	GATE1*	Low
4	SUPV+	High
4	BGC*	High
4	DCNTCS*	Low

During a write, D15 is set to 1 to enable DMA and to a 0 to disable DMA. D14 is IDMAR/W; it is set to 1 for a DMA read and to 0 for a DMA write. Each time D15 goes from 0 to 1, a DMA disk request is generated. Since this is done before a Read/Write Sector command, the data transfer is invalid. If the request is for a DMA write, a transfer occurs to the current address in the DMA address counter. Thus the DMA address must be loaded before the DMA count so that the write goes to a known memory location. Data bits D0-D13 are loaded with the 2's complement of the number of words to be transferred.

Loading WD1010 Task File Registers

These registers must be loaded with information such as sector count, sector number, cylinder number, and command. The processor accesses the task file registers by running a slow bus cycle. The processor asserts chip select to the WD1010 by accessing port E0000X, where X is the address of the target task file register.

The status of address bits PA16-PA23 during the loading of the task file register is:

PA23	PA22	PA21	PA20	PA19	PA18	PA17	PA16
1	1	1	0	0	0	0	0

The signal sequence to assert the chip-select of the WD1010 controller follows:

Sheet 3:

- o Gate 27F (pin 12) generates I/ORQ+ since PDS+, SPA23, and INTA* = 1.

Sheet 9:

- o I/ORQ+ causes the DMA address IC to assert BGACK* (refer to gate array schematics, sheet 5 of 6).
- o I/ORQ+ feeds pin 1 of 1F, which outputs low to 6A. 6A steers F/F 4A to set on the next 1PCK+, generating BGACK*.
- o I/ORQ+ also feeds pin 3 of F/F 5B. BGACK+ removes the reset from all of the 5B F/Fs. The slow-cycle timing chain now begins its cycle.
- o I/O DTACK+ is asserted by F/F 4B 650 ns after BGACK+.
- o Gate 6A (pin 8) has been serving as a latch for BGACK*. When the timing chain has run its course (800 ns after BGACK+), F/F 5B (pin 19) disables 6A and BGACK is dropped at the next 1PCK+.
- o Gate 7A (pin 8) is used when writing to the disk controllers, and gate 3B (pin 6) is used when reading from the disk controllers.

Sheet 6 of 6:

- o Logic element 8G is the command transceiver. It is enabled by DCS*, which is HDCS* ORed with FDCS*. 8G transfers data between the system bus and the disk data bus when the processor is communicating with the disk controllers.

Logic Board Theory of Operation

Sheet 17:

- o Decoder 6J is enabled by BGACK* and asserts I/OEN*.

Sheet 4:

- o Decoder 27G is enabled because BGC* is inactive, SUPV+ is active, I/OEN* is active, and address bit A21 = 1.
- o A16, A17, and A18 are all equal to 0, causing 27G to assert HDCS*.

Sheet 11:

- o The WD1010 is being addressed by bits 1-3 from the system address bus. The data is on the DD bus from the DMA data IC.
- o All that is required to write data to the addressed task file register is HDCS* and WR*.

Executing Hard Disk DMA Read

Listed below are signal exchange sequences that occur during a disk DMA Read Sector command. The first sequence begins the cycle, and the rest repeat until a complete sector of data has been read from memory to disk.

Reading Sector Signal Cycles

The cycle begins with a Write Sector command:

- o The 68010 writes the Write Sector command to the WD1010 controller.
- o The controller responds to the Write Sector command by generating HDBCS* (pin 1), shown on sheet 11. This signal is generated every time the disk controller is ready to receive a byte from the disk DMA bus interface.
- o The disk PAL on sheet 2 responds to HDBCS* by asserting TFER* (transfer request). This first transfer request begins the following repeating cycles:

Repeating signal exchange between DMA interface and the arbitration PAL:

- o The DMA data array responds to TFER* by asserting DKRQ* (disk bus request), shown on sheet 10. DKRQ* is the request to the bus arbitration PAL for a disk DMA machine cycle. Because the disk DMA bus interface receives 16-bit words from memory and the disk controller receives 8-bit bytes from the DMA data array, DKRQ is asserted once for every two times that TFER* is asserted.
- o The arbitration PAL on sheet 2 responds to DKRQ by asserting DKBG*.
- o The DMA address array responds to the bus grant by asserting BGACK.
- o After 200 ns, the DMA address array negates BGACK.

Repeating signal exchange between disk DMA bus interface and the bus:

- o When DKBG* is asserted, the DMA address array loads the DMA address on the bus. Each time the address is loaded on the bus, the address counter in the address array is incremented.
- o When BGACK* is asserted, the DMA data array loads DMA data on the bus. A 16-bit word is read into the word buffer in the data array from RAM memory.
- o When DKBGA* is negated, both address and data are removed from the bus to complete the machine cycle.

Repeating signal exchange between DMA interface and the disk controller:

- o When TFER goes high, the lower half of the 16-bit word stored in the DMA word buffer is transferred by the DMA data array to the disk controller.
- o The next time TFER goes high, the upper half of the 16-bit word stored in the DMA data array is transferred to the disk controller. A new bus request is generated by the DMA data array, causing a new word to be written into the word buffer of the DMA data array.

Logic Board Theory of Operation

Repeating memory access via arbitration PAL:

- o Each time DKBG* is asserted, the arbitration PAL asserts BGC+.
- o On sheet 3, BGC+ causes the assertion of ENRAS*, which starts the memory timing sequence.

Controller interrupt ends command execution:

- o When the last byte has been written to disk, the controller asserts HDINTRQ, interrupt output pin 3. Sheet 15 shows this signal connected to the line printer status register. If the program is using polling, this register is read to detect command completion. If polling is not used, the interrupt (see sheet 6) generates a level 2 interrupt.

Terminal Count

Terminal count is reached when the DMA count register toggles from FFFF-C000. This means that the programmed number of words has been transferred. (Refer to DMA data IC on sheet 6 of 6.)

- o When counter 7C contains FF and counter 7D contains FF, pin 14 of 7D goes low the next time the counters are clocked. This feeds pin 2 of 4E and pin 13 of 2B. 2PCK+ clocks 2B clear and pin 15 outputs low to the D input of F/F 2B. The following 2PCK+ clocks this F/F clear and TC* is generated.
- o TC* is tied to pins 1 and 10 of 1D. This disables 4D and no more disk bus requests are generated.
- o The processor is informed of the completion of the disk operation by an interrupt from the disk controller. HDINTRQ+ is generated by the WD1010 upon completion of a command.

If interrupts are being masked by the processor, such as during the bootstrap routine, the interrupts can be detected by polling the line printer status register (bit 2), address 470000.

Underrun/Overflow Errors

An underrun condition occurs when the DMA cannot send bytes to the disk controller fast enough. This is an error condition associated with a disk write operation. An overrun occurs during a disk read operation when the DMA cannot read bytes from the disk controller fast enough.

The disk controller transfers data to and from a disk spinning at a fixed speed (+ or -1%) and a minimum of 512 bytes must be moved during a Read/Write Sector command. Thus the disk controller must read or write a byte when it is under the head in the drive. The drive motor cannot speed up or slow down for some other bus master to get off the bus. Thus bus arbitration gives highest priority to disk DMA; otherwise an underrun/overrun error could occur (sheet 6 of 6).

- o F/F 4C (pin 5) asserts the U/OERR. This F/F is clocked each time the DMA requests the bus. The D input is high if the DKBCA* signal is still active. Therefore, if the DMA requests the bus while a disk bus grant is still active, a U/OERR is generated.
- o The error is detected by the processor by sampling bit 15 of the DMA count register, address 460000.

Separating Hard Disk Data

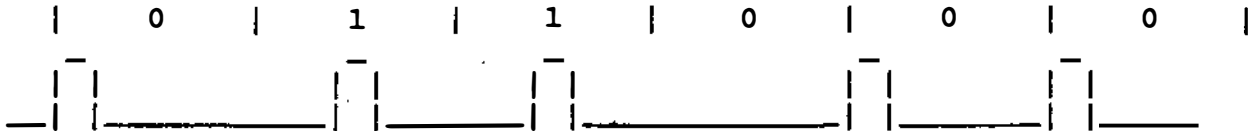
Data separation is accomplished by a combination of a VCO, phase detector, and a loop filter. These are called the data separation circuits and they operate as described below.

Modified Frequency Modulation (MFM)

MFM is the method used to encode serial data written on disk. This method allows the disk controller to distinguish 1's from 0's when the data is read back. Encoding is done by positioning pulses at the beginning or middle of a sequence of 200-ns bit cells, one cell for each binary bit to be written. No more than one pulse can be written in each cell, and certain cells will be empty. A pulse at the beginning of a cell indicates a 0 bit stored in that cell, and a pulse in the middle of the cell indicates a 1 stored in that cell. An empty cell indicates a 0 preceded by a 1. In this last case, the previous cell must contain a pulse in the middle, which ensures that the time between pulses is always equal to or larger than one cell time. The pulse at the beginning of the cell also serves as a clock pulse. When data is read back, a phase locked loop (PLL) is locked to this pulse. The width of the bit cell is fixed by the speed of the disk drive motor, which is 200 ns for the hard disk. The alignment of the bit cell with respect to the data is maintained by the phase-locked loop. An example of MFM coding follows.

Logic Board Theory of Operation

200-ns Bit Cells



- o An 0 is written at the beginning of a bit cell; 0's also serve as clocks.
- o A 1 is written in the center of bit cells.
- o A 0 following a 1 is not written because the flux density on the media would be too great. MFM data bits must be separated by at least one bit cell. If a bit cell is empty, the controller knows that it must have been a 0 following a 1.

Data Separation Circuits

The circuits that make up the data separator are:

- o Voltage-controlled oscillator (VCO) (IC 14N)
- o Phase detector (output at IC 18M, pins 11 and 8)
- o Loop filter (output at IC 17N, pin 1).

Voltage-Controlled Oscillator

During a Read Sector command, the VCO is phase locked to the incoming data. Pin 1 is the voltage control pin. When pin 1 is 0 volts, the oscillator output frequency is about 3 MHz. When it is 5 volts, the output frequency is about 18 MHz.

Phase Detector

The phase detector includes the two data flipflops in IC17M, whose outputs are labeled REF and VAR. The REF and VAR F/Fs are used to compare the reference frequency to the variable VCO frequency. NAND gate 18M is connected so that, when REF and VAR are not both set or reset, a pullup or pulldown pulse is generated. At the beginning of a cycle, both REF and VAR are low.

If the frequency of the PLL is too high, the PLL clock goes high at pin 3 of 17M before the delayed reference at pin 11 of 17M goes high. In this case, 18M pins 9 and 10 are both high and a pulldown pulse is generated to pull the frequency back down.

If the frequency of the VCO is too low, pin 3 of 17M goes high after pin 11 of 17M goes high. In this case, pins 12 and 13 of 18M are both high, generating a pullup pulse at 11.

In either case, following pulses set whichever flipflop is not set first, and then reset them both.

Loop Filter

Operational amplifiers (17N) implement a loop filter. The filter is slow in responding to the error pulses produced by the REF and VAR F/F's and prevents the VCO from reacting to random phase differences. A pullup pulse turns on Q7, which makes the junction of R68 and R67 +5 volts. This makes the output of 17N at pin 7 swing negative at a rate dependent on the value of C253 and R68.

Pin 7 of 17N is connected to the input of an operational amplifier whose output is 17N at pin 1. This operational amplifier is configured as a 2:1 inverting amplifier. Its output is connected to the voltage control pin 1 of the VCO. RP24 adds a positive bias to the output of 17N so that, if pulldown is grounded, pin 1 of the VCO drops to a minimum of 0 volts. If pullup is grounded, pin 1 of the VCO goes to a maximum of +5 volts.

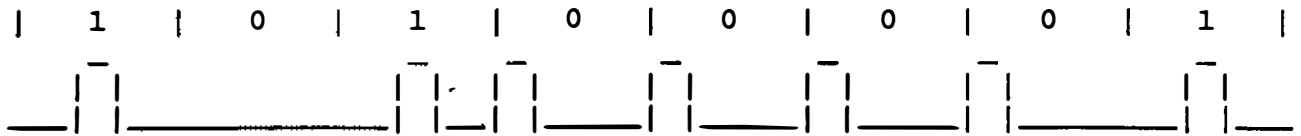
Finding a Valid Address and Data Mark

Beginning the ID field and preceding the data field of a disk sector, there are 14 bytes of 0's. This string of 0's is used by the read circuitry to synchronize the read clock with the read data (remember, 0's double as clocks).

After the 14 bytes of 0's, there is a byte containing A1. This byte is used to validate the 0 string. It is not impossible to have 14 bytes of 0s followed by a byte containing A1 as data. Therefore, to guarantee that the 0's preceding an ID field are indeed marking the beginning of an ID field, a trick is performed on the byte containing A1:

Logic Board Theory of Operation

200-ns Bit Cells



This example illustrates the special byte following the 0 string (A1). Normally, a 0 following a 1 is not written; in this case, however, the rule is broken. Notice that in the second instance of a 0 following a 1, the 0 is written. This is the only time that this is true. It guarantees that the preceding 14 bytes of 0's are truly marking an ID field.

The DRUN signal shown on sheet 12 is used to detect strings of 1's and 0's. DRUN is high during a continuous string of either 1's or 0's. It goes low if a data stream that contains both 1's and 0's is present.

The WD1010 checks DRUN during a Read or Write Sector command. HDRGATE is an output of the WD1010 controller. It is set high when the WD1010 is inspecting data. When HDRGATE is high, the DRUN one-shot input is connected to data from disk. When HDRGATE is low, the DRUN one-shot input is connected to PCK.

These signals are used when the WD1010 is searching for a valid address and data mark. When the WD1010 starts executing a read sector command, it sets HDRGATE low and checks DRUN. DRUN must go high since PCK will look like a continuous string of 0's. The WD1010 sets HDRGATE high and checks DRUN.

If DRUN goes low within five byte times, the WD1010 resets HDRGATE and the sequence starts over. If DRUN remains high for five byte times, the WD1010 starts searching the data for an address mark. If DRUN goes low during this search, the WD1010 deasserts HDRGATE and the sequence starts over.

If an address mark is found, a similar search for a data mark begins. If a data mark is found, the sector is read.

If both address and data marks are not found within eight index pulses, bit 4 in the error register at E00002 is set and the command is aborted.

Write Compensation

The write compensation circuitry is shown on sheet 12. These circuits are used when data is written to disk. They compensate for timing errors that would otherwise occur when data is written to inner sectors.

In the inner sectors, the distance between bit cells is reduced. If not compensated for, the read pulse produced by a bit in one cell will reduce the time between it and the read pulse produced by the bit in the next cell. To compensate for this, the time between pulses during write is increased. The signals EARLY* and LATE* control the delay. Associated circuitry is described below:

- o The write data is synchronized with PCK+ at latch 16K. It then feeds the D input to F/F 16M.
- o The hard disk separator PAL (14M) outputs a signal named MUX on pin 19. During a write operation, MUX has the same phase and frequency as PCK*.
- o Since MUX is derived from PCK* in this case, it is a 10-MHz signal. MUX is tied to the clock input (pin 11) F/F 15K.
- o This signal inputs to a 50-ns, multitap delay line. Pin 12 is the 10-ns tapoff, pin 4 is the 20-ns tapoff, and pin 10 is the 30-ns tapoff. These outputs are tied to one of four decoders 14K. The 20-ns tapoff also clears F/F 15K.
- o The select inputs of 14K are tied to LATE* and EARLY*. These two signals decide how long to delay the data, as dictated by the write precompensation circuitry in the WD1010.

Floppy Disk Direct Memory Access

The Western Digital WD2797 performs the functions of the floppy disk controller/formatter. This device contains a high-performance phase-lock-loop data separator and write precompensation logic. An on-chip VCO and phase comparator allows adjustable frequency range for 5.25-inch and 8-inch floppy disk interfacing.

Pin Functions (Sheet 13) for the WD2797 are listed in Table 2-24.

Table 2-24 Pin Functions WD2797

Pin(s)	Signal Description
7-14:	D0-D7; eight bidirectional buses used for transfer of commands, status, and data.
5-6:	A0-A1; these inputs select the register to transmit/receive data on the data bus under control of WE-/RE-.
4:	Read-enable; a low on this input controls the placement of data from a selected register on the data bus when CS is low.
2:	Write-enable; a low on this input gates the data on the data bus into the selected register when CS is low.
3:	Chip-select; a low on this input selects the chip and allows computer communication with the device.
22:	Test; a low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.
27:	Read data; digitized read back of the flux reversals on the floppy disk.
32:	Ready; because of strapping, this signal goes low when the door is closed and the drive is selected; it goes high when the door is open and the drive is selected. The 2797 disk controller does not interrupt the processor when the ready signal changes states, so the processor must poll the controller periodically to determine when a floppy disk has been mounted or dismounted.
34:	Track 0; asserted by the selected drive when the head is positioned over track 0.

Table 2-24 Pin Functions WD2797 (Continued)

Pin(s)	Signal Description
35:	Index; asserted by the selected drive when the index hole is passing over the index sensor. This signal pulses every 200 ms and has a nominal duration of 4 ms.
36:	Write protect; asserted by the selected drive to indicate that a write-protected floppy disk is mounted.
23:	Pump; high-impedance output signal that is forced high or low to increase/decrease the VCO frequency.
26:	VCO; an external capacitor tied to this pin adjusts the VCO center frequency.
15:	Step; pulsed low by the controller to move the head one track in the direction indicated by the direction signal. The 2797 disk controller issues one step pulse every 3 ms. The drive ignores step pulses that would force the head to a negative track number or beyond track 79. The drive also ignores step pulses that occur when write enable is active or the select line is inactive.
16:	Direction-select; driven low by the controller when stepping to a larger track number; driven high when stepping toward track 0.
25:	Side-select; when driven low by the controller, head 1 is selected; when driven high, head 0 is selected.
29:	Track greater than 43; enables write precompensation for tracks 44-76.
28:	Heads load; controls the loading of the read/write heads against the media.

Table 2-24 Pin Functions WD2797 (Continued)

Pin(s)	Signal Description
30:	Write gate; enables the write circuits on the drive, provided the floppy disk is not write protected.
31:	Write data; MFM or FM output pulse per flux transition. WD contains the unique address marks as well as data and clock in both FM and MFM formats.

WD2797 Registers

The WD2797 has the following internal registers that must be programmed before disk operations:

Table 2-25 WD2797 Registers

Address	Read Information	Write Information
E10000	Status register	Command register
E10002	Track register	Track register
E10004	Sector register	Sector register
E10006	Data register	Data register

WD2797 Commands

The WD2797 floppy disk controller executes a total of 11 commands. It does not have the implied seek function of the hard disk controller, but it does have a Read Track command that allows examination of an entire track of data for debugging purposes. The commands are listed in Table 2-26.

Table 2-26 WD2797 Commands

Command	Function
Restore	Moves heads to track 0
Seek	Steps heads to track number in track register
Step	Moves heads one step in same direction as last
Step-in	Moves heads in one track
Step-out	Moves heads out one track
Read Sector	Reads one or multiple sectors--aborts if error
Write Sector	Write, same as read
Read Address	Reads first ADX mark and ID field past index
Read Track	Reads track, reports errors--no abort
Write Format	Formats system, provides data for gap and ID
Force Interrupt	Drives interrupt line

Logic Board Theory of Operation

Initializing Floppy Disk Write

The following list describes the operations a program must perform to initialize the system before sending a Read Sector command to a disk controller:

Loading System Disk Bits and DMA Interface

- o Selects the drive by writing to the disk control register.
- o Loads the DMA address registers with the starting logical address. (The address is incremented from low memory to high memory.)
- o Loads a 0 to D14 (DMAR/W-) of the miscellaneous register.
- o Loads the DMA count register with DMAEN+ = 1, IDMAR/W- = 0, and the 2's complement form of the number of words to be transferred. This causes an invalid transfer of one word and thus requires the reloading of the address register.
- o Reloads the DMA address register with the starting logical address.
- o Reloads the DMA count register with DMAEN+ = 1, IDMAR/W- = 0, and the 2's complement form of the number of words to be transferred.

The reason for reloading the DMA address register and the DMA count register is that, when the DMA count was initially loaded, the DMAEN+ bit was toggled from low to high. This generates a false disk bus request, and the system does a DMA write to memory. The transfer is false because we have not yet received any bytes from the disk controller. Whatever was latched in the disk buffer was written to memory.

The U/OERR- (bit 15, read) in the DMA count register indicates an underrun or overrun has occurred. With the current bus bandwidth and the priority setting of the bus masters, disk DMA should not experience any underrun or overrun error in any bus traffic condition.

Setting Up the Disk Controller

- o Loads the controller registers with the desired sector and track number using the disk data bus DD0-DD7.
- o Writes the Read Sector command to the disk controller. Execution of the DMA read begins as soon as the controller receives this command.

The same DMA circuit is being used with the floppy disk as was used with the hard disk. The DMA count register and the DMA address register are loaded in the same manner as discussed earlier.

The major difference between the disk write operation discussed earlier and a disk read operation is that, with a read operation, data is transferred from the disk in bytes, assembled into words at the disk buffer, and written to memory.

Executing Floppy Disk Write

Once the DMA has been set up and the WD2797 has been commanded to read, the floppy controller finds the programmed sector and begins to read the MEM data. It then converts the MEM data into binary data and assembles a byte. The byte is placed in the 2797 data register, and a data request is presented to the system.

Sheet 13:

- o Read data is input to the floppy controller on pin 27. When a byte has been assembled, the 2797 asserts FDDRQ+ from pin 38.

Sheet 2:

- o FDDRQ+ is tied to the D input of F/F 16K. This is an asynchronous signal that is synchronized with the system by 1PCK+ generating FDDRQL+.
- o FDDRQL+ inputs to the disk PAL 24H. The PAL generates TFER*.
- o FDTFER* starts a timing sequence; QB* is generated on the 1PCK+ following FDTFER*, the next 1PCK+ generates QC*, and the next 1PCK+ generates QD*.

Logic Board Theory of Operation

- o TFER* goes active at QB* time and generates FDRE*; TFER* and FDRE* remain active until QD* time.

Timing diagram, Figure 2-3, shows the relationship between the preceding signals:

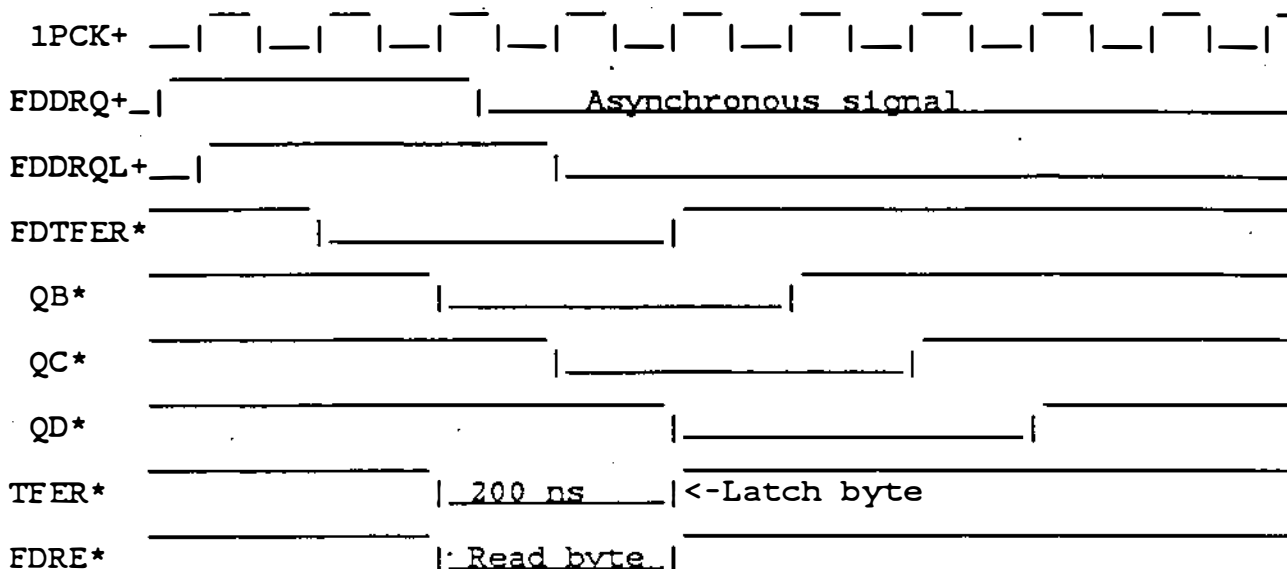


Figure 2-3 Floppy Disk Write Timing Diagram

Sheet 13:

- o Chip-select* (pin 3) on the WD2797 is tied low. FDRE* causes the controller to drive the byte onto the DD bus and to disable FDDRQ*.

Now that there is a byte of data on the DD bus, the DMA circuitry must latch the byte in the stacking portion of the data buffer. The DMA waits for another byte and stacks it with the first byte, forming a word. Then a disk bus request is generated. When the bus grant is received, the word is written to a memory address specified by the DMA address counter. (Refer to sheet 6 of 6 in the gate array schematics.)

As mentioned earlier, the first DMA transfer is a false write to memory.

The following sequence describes the generation of DKRQ*:

- o Gate 1D pin 10 is high as long as it is not terminal count. Pin 9 is high because F/F 4A is previously clear. Pin 13 is high because we are doing a DMA write. When the DMA is enabled by setting bit 15 in the DMA count register, pin 12 goes from low to high.
- o This causes a low to high transition on 4D pin 8, which clocks pin 11 of F/F 4C. The F/F clears and pin 9 goes low.
- o The low from pin 9 forces a high from gate 1E pin 3. Pin 3 is tied to the D input (pin 12) of F/F 1C. The trailing edge of the next 2PCK+ clears this F/F, generating DKRQ*.

At this point the software is reading the DMA count register until it is incremented. This is done to tell when this false transfer has been accomplished. After the software has determined that the count register has incremented, the DMA address register and count register are reloaded. Then the controller is issued a command sequence, and a genuine DMA write operation begins.

- o F/F 4A is clear initially (inactive DMAEN+). The Q output is low, partially enabling 4E. TFER* fully enables 4E (pin 13) and pin 11 is driven low.
- o TFER* is a 200-ns signal. When it goes inactive, pin 11 of 4E goes from low to high. This latches the byte in the high byte of the buffer and toggles the TFER F/F (4A) set.

The DMA waits for another request (FDDRQ+) from the controller. When the controller requests, the disk PAL again asserts FDRE* and TFER*. FDRE* reads the next byte, which is latched in the low byte of the data buffer when TFER* goes inactive.

- o When TFER* goes inactive, the TFER F/F toggles from set to clear. This enables pin 9 of gate 1D (the other pins are still enabled as before), which causes a legitimate DKRQ.

From this point, the operation proceeds the same as the DMA read operation, except that the data is going in the opposite direction.

Video Bit Map

The video circuits appear on two sheets of the schematics. The circuits on sheet 8 contain bit map memory IC's 14-17 and video shift register IC's 14-15. Composite video is output from these circuits to the monitor at IC26B (pin 8). The video gate array is shown on sheet 7 and on sheets 2 and 3 of 6. The gate array generates timing and control signals, including vertical and horizontal synchronization for the composite video and bit map address and read/write control signals for the bit map memory. Composite video is an analog signal that contains both synchronization and picture information.

Screen Layout

Video is bit mapped. The screen is divided into thousands of points. Each point is assigned an address and a binary value of 1 or 0 in a 16-bit word. These words are stored in bit map memory. Adjacent points are grouped together so they can be stored in the same 16-bit word.

To create a display, an electron beam scans the screen as shown in Figure 2-4, moving from left to right and top to bottom. The display produced in this way is called a raster scan, and each picture produced is called a field. The bit map memory holds one field; 60 fields per second are produced.

The relationship between bit map address and screen position is shown on the next page. At the beginning of a scan, the beam points to the upper-left corner of the screen. The contents of address 420000 are loaded into a 16-bit shift register. As the beam moves from left to right, the contents of the shift register are shifted out to the monitor. If the current bit is a 1, the beam is on and a point of light appears on the screen. If it is a 0, the beam is turned off and the screen is dark at that point. The horizontal sweep circuit moves the beam to the right until it reaches the right side of the screen. Then the horizontal sync pulse causes the horizontal sweep circuit to swing the beam back to the left side of the screen to start the next horizontal sweep.

At the same time that the horizontal sweep circuit is causing the beam to scan from left to right, the vertical sweep circuit is causing the beam to move from top to bottom. The rate of vertical sweep is such that the beam moves down the screen the width of one line for each horizontal sweep.

When the last bit is displayed in the lower-right corner of the screen, the vertical synchronization pulse and the horizontal synchronization pulse turn on. This causes the beam to return to the upper-left corner to start the next field. In the UNIX PC raster, there are 348 horizontal lines, each line containing 720 bits. Each point is called a pixel. Thus, there are 720 x 348 or 250,560 pixels.

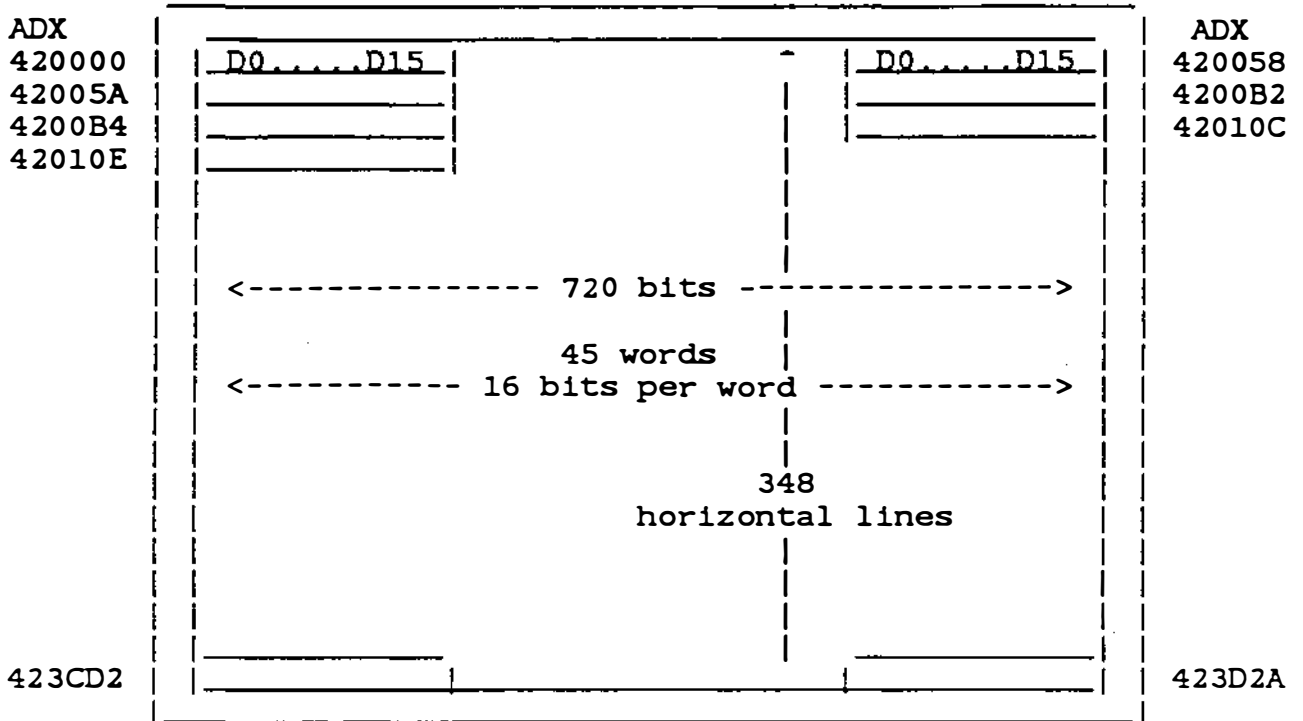


Figure 2-4 Screen Layout

Bit map memory is composed of dynamic RAM. Reading and displaying an address serves a dual purpose of refreshing and displaying the contents of the bit map. The UNIX PC allocates 32 KB of system address space for the bit map. This is implemented by a 16K x 16 dynamic RAM array. The screen layout above illustrates how the processor must address the bit map. Data written to address 420000 produces the pixels on the first line at the upper-left portion of the screen.

Logic Board Theory of Operation

The refresh circuit reads 16-bit words from the bit map, addressing the bit map with an address counter. It then loads the word into a shift register and shifts it out at the speed of a 20-MHz pixel clock. This creates a serial video stream. A 20-MHz clock has a cycle duration of 50 ns, so one word is shifted out every 800 ns. There are 45 words in each row. The refresh logic reads them consecutively and shifts them out to the deflection board.

After all of the pixels on a line have been displayed, horizontal retrace occurs. This lasts 11 word times or 8.8 us. Vertical retrace lasts 1079 word times. The beam must be turned off during retrace to prevent diagonal retrace lines from appearing on the screen. If the intensity is turned up too high, retrace lines may appear even though the composite video signal from the motherboard is correct.

State Generator

The state generator circuit is shown on sheet 2 of 6. The state generator produces four state signals: S0-S3, see Figure 2-5. These signals generate timing signals that allow the 68010 to write to the bit map and the refresh address generator to read. The effect is such that a person looking at the screen is not aware of the loading operation. The screen appears to change instantaneously.

Four F/F's (S0-S3), IC2G, and 3J generate the state signals. They constantly repeat the same sequence of state conditions shown below. Each state lasts 50 ns clocked by the 20-MHz signal. Each state is given a number by assigning binary weight values to the state signals: S0 has a weight of 1, S1 a weight of 2, S2 a weight of 4, and S3 a weight of 8. Thus each 50-ns period has a state value, calculated by adding weights, that repeats over and over. The period of 0-50 has a state value of 1. The period of 50-100 has a value of 3. Thus the repeating sequence of state values is 1, 3, 7, 15, 14, 12, 8, 0.

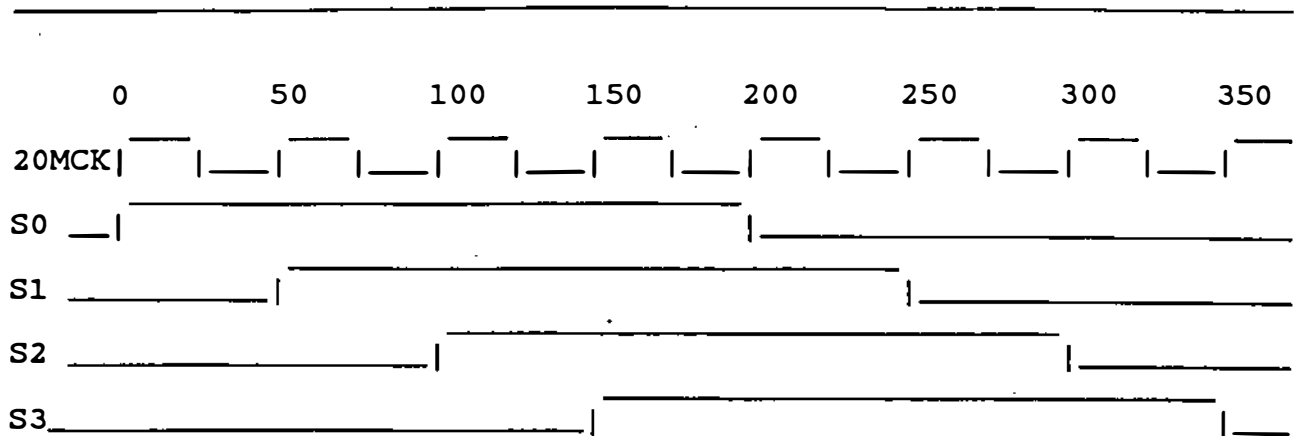


Figure 2-5 State Signal Generator Timing

These states are used to perform the following timing functions:

- o Generation of a signal called BMWINDOW, which allows the 68010 and the refresh address counter to write to the bit map by switching the select input to the address multiplexer.
- o Generation of BMRAS (bit map row address strobe) and BMCAS (bit map column address strobe) signals to load and refresh 68010 row and column address into the bit map.
- o Generation of BMACK, which in turn generates DTACK to tell the 68010 to finish a bit map write machine cycle.
- o Generation of SRLD to load 16-bit words from the bit map into the shift register.

68010 Loading of Bit Map

32 KB of system address space is allocated for the video bit map, addresses 420000-427FFF. When the processor needs to alter information on the monitor, it does so by loading data into the video bit map RAM chips. The processor must be in supervisor mode to do this. The following discussion describes a 68010 write operation to the bit map.

First the signal BMSEL (bit map select) is generated by address decoding. This signal tells the video array that the 68010 wants to address the bit map. The signals to generate BMSEL are listed in Table 2-27.

Table 2-27 Signal Status to Generate BMSEL

Sheet	Signal	Status
17	SPA23	0
17	PA22	1
17	GATE1*	0
4	PA16	0
4	PA17	1
4	PA18	0
4	PA19	0
4	BGC*	1
4	SUPV	1

On sheet 2 of 6, a signal called CCK is combined with the output of flipflop 2F (pin 6) to generate BMWINDOW*. The F/F 2F (pin 9) is set for one cycle through the states and cleared for the next cycle. It keeps toggling with every cycle, so it generates CCK every other cycle through the states.

CCK switches the video RAM address input between the processor and the raster refresh circuitry. This is done by the output of IC 1F (pin 8). When 1F (pin 8) is low, multiplex chips select address input from the system address bus. 1F (pin 8) is low when CCK* and 2F (pin 6) are high. 2F (pin 6) is clocked high within 800 ns after BMSEL* goes low.

A processor reference to video RAM can be a fast cycle (400 ns), but if CCK is active when BMSEL* arrives, the processor has to wait until the next cycle of states. For the longest possible cycle, it could take the processor 800 ns to reference the bit map.

Gate 1F (pin 8) low switches address multiplex chips IC2J, 2K, 2L, and 2M so that bit map address output BRA0-BRA7 is loaded from address bus A1-A14. BMACK+ is generated at S3 (150 ns) and is used on sheet 2 to assert DTACK* to the 68010 to complete the machine cycle.

BMWINDOW* enables bit map data transceivers 13A and 17B on sheet 8. It also gates the R/W* signal through 26F, creating BMR/W*. The direction of the transceivers is controlled by R/W*. For our discussion, that signal will be low, causing the transceivers to pass the data from the system data bus to the bit map data bus.

On sheet 8 the bit map is set up for a read operation unless the 68010 is performing a write. Gate 26F controls bit map read/write (BMR/W*) at pin 3.

BMRAS* and BMCAS* strobe in the address, and the data is output 120 ns after RAS is asserted.

Bit Map Address Multiplex

The bit map address MUX's are 2J, 2K, 2L, and 2M. They select an address from the system address bus when the 68010 is accessing the bit map, or they select the address from the refresh address counter (1K, 1L) during raster refresh.

The MUX's output row address when S2 is low and column address when S2 is high. In other words, the row address is gated until the 100-ns mark, and then the column address is gated. Tables 2-28 and 2-29 illustrate which address bits are selected and the functions of these bits with respect to the select inputs (A and B) of the bit map address MUX's:

Table 2-28 Multiple Select Status

B	A	Function
0	0	68010 row address
0	1	68010 column address
1	0	Refresh row address
1	1	Refresh column address

Table 2-29 Bit Map Address Multiplex Assignments

B	A	7	6	5	4	3	2	1	0
0	0	A14	A13	A12	A11	A10	A9	A7	A6
0	1	GRND	A6	A5	A4	A3	A2	A1	GRND
1	0	BA14	BA13	BA12	BA11	BA10	BA9	BA8	BA7
1	1	GRND	BA6	BA5	BA4	BA3	BA2	BA1	GRND

The row address and column address strobe signals are generated as described below on sheet 2 of 6.

Gate 2E (pin 6) enables RAS and CAS. Pin 5 is used during a 68010 reference and pin 4 is used during screen refresh. Gate 1J (pins 3 and 5) is enabled by S1 and/or S2, and it outputs BMRAS* at 50-300 ns. Gate 1J (pins 9 and 13) is enabled by S0 and/or S3, and it outputs BMCAS* at 150-400 ns. Gate 2E (pin 6) enables the 1J gates to generate BMRAS* and BMCAS* when CCK+ is high, as previously described (BMRAS* at 50-300 ns, BMCAS* at 150-400 ns).

On sheet 8, IC's 14A, 15A, 16A, and 17A are 16K x 4, 120-ns dynamic RAM chips that compose the bit map.

BMRAS* strobes in the row address, BMCAS* strobes in column address, and BMR/W* causes the data on the BD bus to be written into memory.

Refresh Address Counter

On sheet 3 of 6, chips 1K and 1L make up a 16-bit binary counter. These logic elements are used as the refresh address counter, which addresses the bit map during a refresh operation. The counter is incremented at the end of each video window when HSYNC* is inactive. HSYNC* is active only during horizontal retrace. The counter is cleared by CLR READD+ at the end of vertical retrace.

The counter generates addresses 0000-4163 hex before it is reset. Addresses 0000-3D2A are valid screen addresses. Addresses 3D2C-4163 are generated during vertical retrace and therefore are not used for obtaining pixels.

Horizontal Synchronization

On sheet 3 of 6, logic element 1G, the horizontal counter, generates the timing for horizontal synchronization/retrace. It is clocked by CCK+. It executes a repeating cycle as follows.

Assume that this counter starts counting from 0 and that HSYNC is high. This starts the horizontal retrace. It is clocked by CCK+ when it reaches a count of 10. Gate 3G (pin 8) outputs a low and resets HSYNC low. When the counter reaches a count of 54, IC1H (pin 8) goes low. This sets HSYNC high and resets the counter, thus starting the cycle over. Note that HSYNC inhibits the bit map address counter during horizontal retrace.

Vertical Synchronization

Gate 1N decodes the selected address bit from the BA bus. It outputs low at address 3D2C. This address is driven from the refresh address counter after the last word has been displayed in the lower-right portion of the screen. At this time, 1N clears F/F 1A, causing the generation of VSYNC+, which marks the beginning of vertical retrace. F/F 1A also disables DISPEN*.

The refresh address counter is not disabled during vertical retrace. It is incremented 1079 times. The highest address generated is 4163H.

Gate 1H outputs low at refresh address 4163H, marking the end of vertical retrace. VSYNC+ is disabled via F/F 2H (pin 2). This flop also generates CLR RFADD+, which resets the refresh address counter.

Shift Register

On sheet 2 of 6, gate 2D (pin 6) generates SRLD* at 300-350 ns. This signal causes the data output from the video RAM's to be loaded into a shift register, IC14B and 15B on sheet 8. The shift register serializes the data, creating the video stream.

Logic Board Theory of Operation

SRLD+ latches the word from the bit map into shift registers 14B and 15B. The data is then shifted out at the speed of 20MCK+, which is sometimes referred to as a pixel clock.

The pixels leave the shift register from pin 17 of 15B. The video stream is synchronized again with 20MCK+ at F/F 18D (pin 2). After the video passes through XOR gate 26B (pin 8), it is routed directly to the CRT deflection board.

Telephony

There are three telephone line connections to the UNIX PC. One is for a user telephone, which is referred to as the handset. The other two are active phone lines, designated L1 and L2. These lines are controlled by circuitry shown on sheet 25.

JPH3 is the handset connector for the user phone. The UNIX PC telephony circuitry supports the following functions:

- o Data transmission--through the SCM 882A modem shown on sheet 26
- o Number dialing--dial network 838A chip on sheet 26; serial dial data generation on sheet 7 (DIALER EN* and DIALER TXD)
- o Telephone line management functions and control signals--through circuitry on sheets 25 and 26 listed below:

Detection of ringing on line 1 or line 2--L1 RING, L2 RING (sheet 25)

Message waiting detection on line 1--MSG WAIT* (sheet 25)

Handset offhook detection--OFF HOOK* (sheet 25)

Line 1 or line 2 on hold--L2 HOLD, L1 HOLD (sheet 25)

Dial-tone detection on line selected for data transmission--DT DET (sheet 26)

Handset line select--HDSET RELAY* (sheet 25)

Modem line select--L1 MODEM, L2 MODEM (sheet 25).

Line Control

Line control circuits shown on sheet 25 are described below. There can be two lines coming in, as well as one handset attached.

Line 1 comes in at location 8C (see guides on margins of schematics). If we follow tip (T/R1) and ring (R/T1), we find that they come into bridge rectifier (CSB1) at 6C. This rectifies the 90VAC ringing signal. The time constant of R35-C240 blocks short pulses. The long ringing time causes opto-isolator 7P to conduct, giving us L1 RING*. This is a status line back to sheet 4/C7, to register 9K, which is available to the CPU as a read-only register at 450000h. The opto-isolator prevents potentially hazardous line voltages from coupling into the circuit.

A similar circuit is at 4D, except that there is no R-C time constant, so that MSG WAIT-* appears with a short pulse. This pulse is so short that it is latched into the status register by an extra flop on sheet 4/C6, so that its presence can be observed by the CPU without a prohibitively high polling rate. The CPU looks for a change in status on this line, rather than a high or low.

Sheet 4/3B is the telephony control register. Unlike the status register, which is four bits read at a specific address, this register is treated as eight addresses, 490000-497000h. PD14 is written to the appropriate addresses to control telephony.

Writing a 0 to 492000h gives HOOK RELAY 1*, which turns on Q14 at sheet 25/D6, energizing relay K1. This connects the primary of the audio transformer T1 across tip and ring, presenting a 600-ohm load to the CO and drawing loop current. Audio is passed through T1, safety limited by CR5, and then down to analog switch 5M.

The DG201 is controlled by inputs from sheet 6/5C, a control register at address E4X000h. A low at pin 1 (A1) causes a bidirectional link from pin 2 to 3 (IN1 to OUT1). Audio then passes to sheet 26/C8 and into the 838A dial/network. The signal L1 HOLD+ at sheet 25/C1 turns on Q4, supplying a 510-ohm path to ground and making line 1 quiet while on hold.

Logic Board Theory of Operation

Most of this circuitry is duplicated for the line 2 interface, with the exception of MSG WAIT*. At 7C, relay K3 determines which line is routed toward the handset, with line 1 being the power-loss default, and K6 at 4B determines whether the handset is attached to the active line. The assemblage at 4C detects current drawn from the line as an indicator that the handset is offhook. If K6 has the handset disconnected from the line, this offhook signal is provided through CR12, at the bottom of K6, which also provides enough voltage so that the handset does not appear dead.

Line control signals are written by the 68010 on sheet 4 by first decoding address bits A16-A23 for status as shown below:

Address Status to Enable Telephone Control Register

23	22	21	20	19	18	17	16	Address bits
0	1	X	X	1	0	0	1	Control register

After status is determined, address bits A12, A13, and A14 are used to address the 74LS138. Processor data bit PD14 then writes a high or low into whichever bit is addressed, as shown in table 2-30.

Table 2-30 Address Status to Select Telephony Control Register

Address Bits				Control Bit Selected
15	14	13	12	
X	0	0	0	HDSET RELAY+
X	0	0	1	LINE SEL2*
X	0	1	0	HOOK RELAY1*
X	0	1	1	HOOK RELAY2*
X	1	0	0	L1 HOLD+
X	1	0	1	L2 HOLD+
X	1	1	0	L1 A-LEAD*
X	1	1	1	L2 A-LEAD*

Table 2-31 shows hex addresses that can be used to write to the telephony control register.

Table 2-31 Telephony Control Register--Address 49X000

Address	Bit	Signal	Description
490000	14	HDSET RELAY+	1 = Handset on line
491000	14	LINE SEL2*	0 = Line 2 select
492000	14	HOOK RELAY1*	0 = Hook relay 1 on
493000	14	HOOK RELAY2*	0 = Hook relay 2 on
494000	14	L1 HOLD+	1 = Line 1 hold
495000	14	L2 HOLD+	1 = Line 2 hold
496000	14	L1 A-LEAD*	0 = Line 1 A-lead connect
497000	14	L2 A-LEAD*	0 = Line 2 A-lead connect

This register is forced with 0's after reset.

Telephony Status Register

Also on sheet 4 is circuitry used by the 68010 to read the status of four line control outputs by loading an address on the system address bus. This enables a buffer that loads the status of these bits on data bus bits D0-D3. The address status to enable this buffer is:

Address to Enable 68010 Line Status Read

23	22	21	20	19	18	17	16	Address bits
0	1	X	X	0	1	0	1	Status

The status bits read and the corresponding processor data bus bits are shown in Table 2-32.

**Table 2-32 Telephony Status Register--Address 450000
(Read Only)**

Data Bit	Description	Signal
00	OFF HOOK*	0 = Offhook
01	L1 RING*	0 = Line 1 ring
02	L2 RING*	0 = Line 2 ring
03	MSG WAIT*	Toggled each time a message waiting pulse is detected

Dialer Interface

On sheet 4 a control signal called TM/DIAL WR* is decoded to enable circuitry used on sheet 7 to load data from the system address bus and to convert it to a serial data stream for the dial network chip on sheet 26. TM/DIAL WR* is asserted when the address bits have the following status:

Address Bus Status to Enable Serial Dial Data

23	22	21	20	19	18	17	16	Address bits
0	1	X	X	1	0	0	1	Status

On sheet 4 of 6, TM/DIAL WR* enables a three- to eight-line decoder inside the video gate array. Address bits A10 and A11 are decoded by the decoder to select one of two functions.

First, if A10 = 1 and A11 = 0, then eight bits of data from the address bus are loaded into a shift register whose output is named DIALER TXD. This is the lower byte.

Then with address bits A10 = 0 and A11 = 1, a load signal loads a second set of eight bits (upper byte) of data from the address bus into a second shift register. This load also starts the shift registers shifting data out at DIALER TXD at the rate of 4800 baud. At the same time, an internal counter is counting. After the sixteenth pulse, the registers are disabled.

Serial Communication

The UNIX PC provides an RS-232-C channel that is capable of making either synchronous or asynchronous serial data transfers.

RS-232 Serial Port

Serial data at the RS-232-C port is converted to parallel data by the Intel 7201 programmable controller.

RS-232-C Signal Levels

Data and clock signals produce -12V on the line and control signals produce +12V. On the TTL side, data and clock signals are at +5V when active and control signals are at 0V when active.

RS-232-C Signals

Table 2-33 lists the signals applied to the DB-25, RS-232-C connector. The list gives the pin number, signal name, and direction with respect to the UNIX PC.

Table 2-33 RS-232-C Signals

Pin	Name	Direction
1	Ground (shield)	Bidirectional
2	Transmit data	Output
3	Receive data	Input
4	Request to send	Output
5	Clear to send	Input
6	Data set ready	Input
7	Ground	Bidirectional
8	Carrier detect	Input
15	Transmit clock	Input
17	Receive clock	Input
20	Data terminal ready	Output
22	Ring indicator	Input
24	DTE transmit clock	Output

Logic Board Theory of Operation

Figure 2-6 shows an example of RS-232-C terminal cable pin assignments.

UNIX PC	Terminal
1	1
2	3
3	2
4-5-6	4-5-6
7	7
8	20
20	8

Figure 2-6 UNIX PC to Terminal Cable Pinning

Standalone Diagnostic Loopback Plug

The standalone diagnostics test RS-232-C functions through the use of a diagnostic loopback plug, which must be installed when a channel is being tested. Figure 2-7 shows the loopback plug pin assignments.

Loopback Plug Pinning

2	3
4	5
4	8
20	6
20	22

(2) Transmit data	---	(3) Receive data
(4) Request to send	---	(5) Clear to send
(4) Request to send	---	(8) Carrier detect
(20) Data terminal ready	---	(6) Data set ready
(20) Data terminal ready	---	(22) Ring indicator

Figure 2-7 Loopback Plug Pinning

Baud Rate Generation

The baud rates are generated in the video IC (refer to the gate array schematics, sheet 4 of 6).

The baud rate generation circuitry consists of binary counters 4F and 3D, latch 4L, and comparitors 4G and 4J.

The baud rate is programmable to provide a wide frequency range (307 KHz-1.2 KHz). The baud rate is selected by loading a value into latch 4L. The latch is loaded when the processor references address 4B0XXX, where XXX is the value to be loaded (the latch receives its data from the address bus). Once the latch has been programmed, the baud rate generation circuit outputs a signal named TMOUT, the resultant baud rate. The frequency is computed using the following formula (where N is a value between 0 and 255, previously loaded into latch 4L):

$$TMOUT = [1/(4 \times N)] \times 1.2288 \text{ MHz}$$

The input to counter 4F is a 614-KHz clock. This frequency is easily divisible to obtain the range of internally generated baud rates.

Comparitors 4G and 4J compare the variable count from counter 4F with the reference count from latch 4L. When the variable count equals the reference count, 4G outputs a high on pin 6. This high is synchronized with the 1.2288 MHz COMMOSC frequency at F/F 3H (pin 3). When this F/F sets, pin 5 outputs a high that clears counter 4F and clocks F/F 3H (pin 11).

The signal generated from pin 11 is the baud rate.

Logic Board Theory of Operation

7201 Serial Controller

The Intel 7201 Multi-Protocol Serial Controller performs all RS-232-C communications control, including serial data in/out, status update, and CPU interrupts. This chip can be used in either interrupt driven mode or polled mode. UNIX PC software uses interrupt driven RS-232-C communications.

7201 Functions

The controller must be loaded with a set of parameters before actual data transfers are executed. Once programmed with data length, parity generation/detection, number of stop bits, and so on, the chip is capable of transmitting bytes written into its data register by the 68010. During receive operations, the controller assembles characters received from the serial line and places them in its data register so the 68010 can read them.

The controller operates in interrupt-driven mode. When a byte is needed for transmission or when receive serial data has been assembled into a byte, the controller interrupts the processor. Upon receiving the interrupt, the 68010 vectors itself to the appropriate RS-232-C interrupt handler (software).

The 7201 controller is shown on sheet 14. The 68010 transfers data to the controller using the lower eight bits of the data bus, and it addresses control registers in the controller using system address bits A1 and A2.

The chip enable and interrupt signals are described later in the "Modem" section.

The controller features two serial channels: channel A interfaces the RS-232-C port, and channel B interfaces the modem.

7201 Clock Selection

The 7201 controller chip is divided into two separate channels. Each channel has the option of communicating either synchronously or asynchronously. If a channel is programmed for synchronous operation, it must use the clock rate produced by the baud rate generation circuitry. If a channel is programmed for asynchronous operation, it can use an external clock provided by the device with which it is communicating. This device is generally a modem.

The TXCKA and RXCKA clocks to channel A are selectable between the TXCK and RXCK clocks, respectively, or the programmable baud rate generator described above.

The output of the baud rate generator is called TMOUT. The select control is controlled by the DTR output at channel B. A 0 selects the RS-232 clock, and a 1 selects the baud rate generator.

The TXCKB and RXCKB clocks to channel B are selectable between the MODEM TXCK and MODEM RXCK clocks, respectively, or a fixed 19.2K-baud generator. The select control is controlled by the MCKSEL bit at the miscellaneous register. A 0 selects the modem clock, and a 1 selects the fixed 19.2K-baud generator.

7201 Registers

Table 2-34 lists addresses that access the internal registers of the 7201 controller:

Table 2-34 7201 Registers

Address	Read	Write
E50000	Ch. A: data read	Ch. A: data write
E50002	Ch. B: data read	Ch. B: data write
E50004	Ch. A: status read	Ch. A: command/parameter
E50006	Ch. B: status read	Ch. B: command/parameter
E68000		Transceiver control 1
E69000		Transceiver control 2
E6A000	Transceiver status	

Logic Board Theory of Operation

Modem

The bandwidth available on a common telephone line supports frequencies of 300-3300 Hz. Since the dc levels 0 and 1 cannot be sent on the telephone line, frequencies representing those levels are sent. This method is called frequency shift keying. The frequencies used must be twice the desired data change rate to be deciphered accurately. They also cannot exceed 3300 Hz, the top of the bandwidth window.

At speeds of 1200 baud and higher, this scheme no longer works, because a frequency above 2400 Hz must be used to signal in one direction and insufficient bandwidth is left for signaling in the other direction, at least not simultaneously. So a method called phase shift keying is used, in which the modem sends out a continuous carrier during transmit time. Data is signaled by changes in the phase of this carrier, rather than its presence or absence. The two modems must be in sync with each other, so that a change in phase can be detected. By using high-quality modems, speeds of 9600 can be obtained, but 300, 1200, and 2400 baud are the most popular.

RS-232 data transmission is described as being either sync or async. Async data has a start bit and a stop bit associated with every character, whereas sync data has phase sync fields at the beginning and end of each burst of characters.

When a modem auto-answers, it is quiet for two seconds, and then it sends a 2025-Hz answer tone. At this point, the originate modem detects the answer tone and responds with a mark signal, either at 1270 Hz, indicating a 300-baud transmission, or 1200 Hz, indicating a 1200-baud transmission.

At 300 baud, the modem transmits full duplex (both directions simultaneously) by dividing the frequency range into two distinct bands, originate and answer. The modem that originates the call transmits 1070 Hz to indicate a space and 1270 Hz to indicate a mark. The modem that answers the call transmits 2025 Hz to indicate a space and 2225 Hz to indicate a mark.

At 1200 baud, the RS-232 data delivered to the modem is still in async format, but data delivered onto the telephone line by the modem is actually sync format. The originating modem sends carrier at 1200 Hz, whereas the answer modem sends carrier at 2400 Hz. Data is indicated by changes in the phase of the carrier.

Modem Bus

On sheet 26 the processor data bus is connected to the modem data bus. The processor data bus loads control data into the modem before data transmission. When data transmission takes place, the 68010 sends parallel data to the 7201 serial port controller, channel B on sheet 14. The serial port then provides serial data to the modem.

The chip select for the modem (MODEM CS*) and the 7201 are generated on sheet 4. The status of data bus bits to address the modem and the 7201 are:

Address Status for Modem and Serial Controller Enable

23	22	21	20	19	18	17	16	Address bus bits
1	1	1	0	X	1	0	1	7201 chip select
1	1	1	0	X	1	1	0	Modem chip select

Bits A23 and A22 are decoded on sheet 17 to produce I/OEN used on sheet 4.

Modem Clock Select

On sheet 14 a signal called MODEM CK SEL* selects clock signals to send to the 7201 serial controller when the serial controller is being used with the modem. MODEM CK SEL* is generated on sheet 15 using system bus data bit D12 and chip-enable signal MREG WR* generated on sheet 3. MREG WR* is part of the miscellaneous control register. It selects the programmable baud rate generator clocks from the modem when low or a fixed 19.2K-baud clock when high.

Address bus status to assert MREG WR* is:

Address Status to Assert MREG WR*								Address
23	22	21	20	19	18	17	16	
1	1	X	X	1	0	1	0	MREG WR*

Logic Board Theory of Operation

Modem Registers

Table 2-35 lists the addresses that access the internal registers of the modem:

Table 2-35 Modem Registers

Address	Read	Write
E60000 E63000 E64000 E65000 E66000		Line control Relay and lamp drivers Options A/S and handshake Options CCITT and disconnect RD, SD control, and chip test

Modem Line Select

On sheet 4 the 68010 writes to the general control register using a control signal called GCRWR* (general control register write) from sheet 4. This signal enables a 74LS259 addressable latch, shown on sheet 6. The latch receives inputs from system address bus bits A12, A13, and A14, which are decoded to select an output. The status of the output is determined by the logic level on 68010 data bus bit PD15. In this way the 68010 can use the status of PD15 to enable the modem line select bits L1 MODEM or L2 MODEM or the dial network control signal D/N CONNECT (dial network connect). These signals listed in Table 2-36 are used on sheet 25.

The status of the system address lines to generate GCRWR* and select a given modem line is:

Address Status to Enable GCRWR*

23	22	21	20	19	18	17	16	Address
1	1	1	X	X	1	0	0	GCRWR*

Table 2-36 Address Status to Select Modem
and Dialer Network Control Signals

Address Bits				Control Written to
15	14	13	12	
X	1	0	0	L1 MODEM
X	1	0	1	L2 MODEM
X	1	1	1	D/N CONNECT

Modem/7201 Signals

Channel B of the 7201 is connected to the modem. The following list describes the usage of the signals associated with channel B:

7201 carrier detect <----- RS-232 ring indicator
 7201 receive clock <----- Modem receive clock/19.2K baud
 7201 clear to send <----- RS-232 data set ready
 7201 transmit data -----> Modem transmit data
 7201 transmit clock <----- Modem transmit clock/19.2K baud
 7201 receive data <----- Modem receive data

In addition to the preceding RS-232 signals, the communications interface also supports the external transmitter clock output, which is pin 24 of the RS-232 connector. This signal is the programmable baud rate generator output.

With the RS-232 DSR (data set ready) and RI (ring indicator) connected to channel B port bits, channel B port bit interrupt should not be used to prevent invalid interrupt being generated by the floating condition of DSR and RI.

Line Printer

There is one parallel printer interface connector on the UNIX PC. It is located at the rear of the machine and is controlled via the printer data register.

Ports

The three input/output ports associated with the parallel printer interface are listed in Table 2-37.

Table 2-37 I/O Ports

Port	Description	Read/Write
4F0000	Line printer data register	Write
470000	Line printer status register	Read
4A0000	Miscellaneous control register	Write

Data on data bus bits D0-D7 are strobed into line printer data register bits PRD1-PRD8.

Control Signals

The printer port is shown on sheet 15 of the schematics.

To send data to the printer, this circuitry performs the following three functions:

- o Sends eight bits of data from the lower eight bits of the system data bus to the 74LS374 eight-bit data buffer
- o Reads the printer status from the 74LS244 eight-bit buffer
- o Responds to interrupts from the printer

Address status to decode LPDATAWR* and LPSTATUS RD* is:

Line Printer Status and Data Address Decode								
23	22	21	20	19	18	17	16	Address
0	1	X	X	1	1	1	1	LPDATAWR*
0	1	X	X	0	1	1	1	LPSTATUS RD*

The line printer is operated through an eight-bit parallel Centronics interface. The line printer interface is interrupt driven and operates in byte mode transfers only.

Write Sequence

The write sequence that initiates the output to the printer is shown on sheet 15 of the schematics. Timing characteristics are shown in Figure 2-8.

Sheet 15:

- o Latch 16P is the line printer data register, address 4F0000. The first step necessary to output to the printer is to write a byte to the data register. This is a normal fast-cycle transfer.
- o The next step is to toggle bit 13 in the miscellaneous control register (27B). The processor must write a 1 to bit 13 and then a 0. This strobes the word to the line printer. LPSTROBE must be active for at least 1 us.
- o When the printer detects LPSTROBE*, it latches the byte and responds with LPACK*. The trailing edge of LPACK* clocks F/F 25H clear and generates LPINT+.

Logic Board Theory of Operation

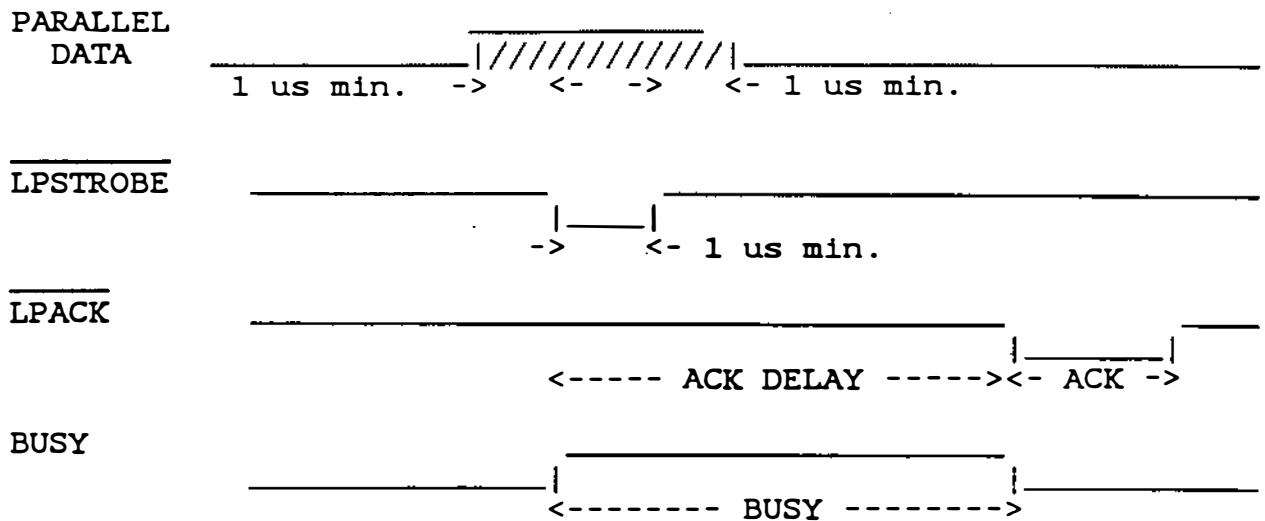


Figure 2-8 Write Sequence Timing

Status Signal Description

Status signals that are sent from the printer to the UNIX PC are listed in Table 2-38.

Table 2-38 Line Printer Status Register--Address 470000
(Read Only)

Data Bit	Signal	Description
07	LPBUSY+	1 = Line printer is busy
06	LPSELECT+	1 = Line printer is selected
05	LPNOPAPER+	1 = Line printer has no paper
04	ERROR*	0 = Line printer error condition
03	FDINTRQ+	1 = Floppy disk controller interrupt
02	HDINTRQ+	1 = Hard disk controller interrupt
01	PERR*	0 = Main memory parity error has been detected; this bit can be cleared with the CSR command (write to 4C0000)
00	DTDET*	0 = Dial tone is detected

The 68010 reads the status of the line printer by asserting LPSTATUS RD*.

Printer Cables

The printer cable pinning is as follows:

Diablo 630 API Cable Pinning

UNIX PC	Printer
1	1
2	3
3	2
4	5
7	7
6-8	20
20	6

UNIX PC to Printer with CTS Control

UNIX PC	Printer
1	1
2	3
3	2
4	4
5	5
6-8-20	
7	7

Figure 2-9 Printer Cable Pinning

Realtime Clock Interface

The realtime clock integrated circuit is the Toshiba TC8250 with power-down battery backup. The TC8250 interface protocol, as listed in Table 2-39, is implemented with software.

Table 2-39 Realtime Clock Interface--Address 480000

Data Bit	Signal	Description
15	RTCCE+	1 = Realtime clock chip enable (write only)
14	RTCALE+	1 = Realtime clock address latch enable (write only)
13	RTCR/W+	0 = Realtime clock read 1 = Realtime clock write (write only)
08-11	RTCD 0-3	Realtime clock data bits 0-3 (write only)
Address E30000 (Read Only)		
00-03	RTCD 0-3	Realtime clock data bits 0-3

Keyboard Controller

The 6850 serial keyboard controller is shown on sheet 14 of the schematics. The keyboard controller alerts the 68010 to read data by generating an interrupt KBINT. The keyboard sends serial data to the controller with a signal called KBTXD. The 68010 then reads data from the controller with processor data bits PD8-PD15. The 68010 enables the controller with KBEN generated on sheet 4. On sheet 4, KBEN is derived from a signal called 6850 CS*, which is decoded from the processor address bits as shown below:

Address Status to Assert KBEN

23	22	21	20	19	18	17	16	Address
1	1	1	X	X	1	1	1	GCRWR*

Table 2-40 lists addresses to access the internal registers of the controller:

Table 2-40 Keyboard Controller Addresses

Address	Read	Write
E70000	Status register	Control register
E70002	Receive data register	Transmit data register

3 Diagnostics

Boot ROM Program

The primary function of the boot ROM program is to boot a program that loads the operating system from the hard disk drive or the diagnostics from the floppy disk drive. In addition, the boot ROM includes a number of diagnostic tests. It tests ROM, RAM memory, and video memory; it also programs the initial status of the memory management hardware and various peripheral controller chips.

During execution, the boot ROM program turns a set of LED's on and off in appropriate binary number patterns as it completes its tests. The LED's are visible through the ventilation slots on the left side of the system. (The ROM test executes so fast that the blinking on and off of the LED's will not be noticed.) The successful completion of each test starts the next. If a test fails, the binary number pattern of that test continues to be displayed as long as the power is on.

Pressing the Reset button or turning on the power causes the boot ROM diagnostics program to execute.

The following descriptions of boot ROM program steps include address and data information for setting up a logic analyzer to trace program execution.

Bootstrap Jump

When the Reset button is released, the initial value of the stack pointer is loaded from addresses 800000 and 800002. The address of the first executable instruction is loaded into the program counter from reset vector locations 800004 and 800006. Then the program:

- o Writes a data word with D15 high to address E40000, which sets IC7K (pin 7) high (ROMLMAP*, sheet 6).
- o Turns off the LED's by writing 0F00 to address 4A0000. (The LED's are controlled by the miscellaneous control register, shown on sheet 15 of the schematics in Section 5.)

Diagnostics

Initializing the System

To initialize the system, the program writes 0700 to address 4A0000, which sets the LED's to binary 1. (Note: Data and address are in hexadecimal notation.)

Initializing the 7201 Serial Port Controller

To initialize channels A and B of the 7201 serial port controller, the program:

- o Sets LEDs to 1.
- o Resets the error registers by writing 18 to addresses E50004 and E50006.
- o Writes F0 to addresses E50004 and E50006.

Initializing the Keyboard

To initialize the keyboard, the program:

- o Resets the keyboard controller by writing 0300 to E70000.
- o Sets the keyboard controller to eight bits per character with one stop bit by writing 9500 to E70000.

Initializing the Modem

To initialize the modem, the program:

- o Disconnects the modem from lines 1 and 2 by writing 8000 to E44000 and E45000.
- o Resets the modem by writing 0001 and then 0000 to E60000.

Initializing the Telephone Line Control

To initialize the telephone line control, the program:

- o Enables the handset by writing 4000 to 490000
- o Selects line 1 by writing 4000 to 491000
- o Reads the telephone status register at 450000.

If bit D0 is a 0, the handset is onhook, so the program writes 4000 to 492000 and 496000 to open relay 1 and line 1.

If bit D0 is a 1, the handset is offhook, so the program writes 0 to 494000 and 495000, and then 4000 to 493000 and 497000, to maintain line 1.

Clearing the Printer Interrupt

To clear the printer interrupt, the program writes 0000 to 4F0000.

Clearing the Dialer Chip

To clear the dialer chip, the program writes 0 to 4B0400 and 4B0800.

Resetting the Disk DMA

To reset the disk DMA, the program writes 0000 to 460000 and 4D0000.

Testing Video RAM

To test video RAM, the program:

- o Sets LEDs to 2
- o Writes 0000 to 420000, the lowest video address
- o Reads the same address (420000).

If the contents are not the same, the program jumps to an error loop. If the contents are the same, the program writes 0001 to address 420002 and continues to read and test.

- o Continues incrementing address and data until the last video memory address (427FFF) has been tested.
- o Reads back each address and checks to see that the contents are correct.

After each address is read, it is written again in case writing to it will affect the contents of the next address.

- o Writes 0000 to all video addresses to clear the screen.

Diagnostics

Testing Map RAM Memory

To test map RAM memory, the program:

- o Sets LED's to 3
- o Performs the same tests on map RAM memory that were performed on video memory from addresses 400000 through 4007FF
- o Sets the unity map by writing to all map RAMs, starting with 400000 and ending with 4007FF
- o Writes A000 to address 400000 to map page 0.

This sets page status bits D15, D14, and D13 = to 101, which corresponds to page status of page present, write enabled, not yet written to, and unity mapped.

- o Increments the address and data and writes to pages 1, 2, 3, and so on until all pages have been declared present, write enabled, not written to, and unity mapped.

Testing RAM

To test RAM, the program:

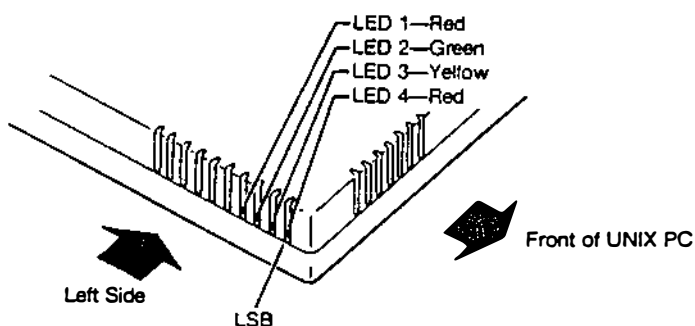
- o Sets LED's to 4.
- o Performs the same memory test as before from addresses 000000 through 7FFFFFFF
- o Sets LED's to 5
- o Sets LED's to 6
- o Puts a small inverse video block on the upper-left corner of the screen
- o Searches for a loader program.

The floppy disk is searched first. If no loader is found or if an error is found, the hard disk is searched. If the hard disk has no loader or has an error (for example, not ready), an inverse video block is added to the screen, and the process is repeated until a loader is found.

Jumping to the Loader Program

When the program finds the loader, it advances the LED's to 7 and the processor jumps to the loader program.

Figure 3-1 shows the LED locations and off/on patterns for each test.



ROM Tests

Test Number	LED Status			
	4	3	2	1
Test 1	Off	Off	Off	On
Test 2	Off	Off	On	Off
Test 3	Off	Off	On	On
Test 4	Off	On	Off	Off
Test 5	Off	On	Off	On
Test 6	Off	On	On	Off
Test 7	Off	On	On	On

Figure 3-1 LED Locations and Off/On Patterns

Listed below is the status of the logic board for each LED test number:

Test 1: Failed telephone initialization
 Test 2: Failed video RAM test
 Test 3: Failed map RAM test
 Test 4: Failed to set map RAM to unity map
 Test 5: Failed dynamic RAM test
 Test 6: Failed initialization
 Test 7: Failed to find loader on disk

Note

Any other failure codes indicate a failure to execute the loader program.

Diagnostics

Floppy Disk Diagnostics

The floppy disk diagnostics are in two parts, a main menu set which exercises the main components of the system, and a subsystem set.

Main Menu Diagnostics Summary

The following list summarizes how the various diagnostic tests from the UNIX PC Diagnostics, Main Menu are divided into subtests or sequences. Tests that require operator evaluation are labeled interactive. The others, which run without user intervention, are labeled automatic. The automatic tests report failures with error messages.

Test 1: Full System Test (Automatic)

This test consists of the following subsystem tests:

Note

These tests are from the subsystem menu, selection 6 of the main menu. They are run in order as listed.

- o Test 2: Floppy disk
- o Test 1: Hard disk
- o Test 5: Memory and parity
- o Test 9: Processor
- o Test 11: Real Time Clock
- o Test 7: Modem

Test 2: Initialize Hard Disk (Interactive)

- o Requests type of drive
- o Formats

Test 3: Enter Bad Blocks (Automatic)

- o Modifies bad block table
- o Displays VHB

Test 4: Park Disk Heads (Interactive)

- o Parks disk

Test 5: Remote Diagnostics (Interactive)

- o Allows diagnostics to be run from a remote site

Test 6: Goto Subsystem Menu

- o These are a series of tests for subsystem checks.

Selection 7: Reboot System

- o Reboots the system.

Diagnostic Subtest Summary

The following list summarizes the diagnostic tests from selection 6 of the main menu. These tests are also divided into subtests or sequences. Tests that require operator evaluation are labeled interactive. The others, which run without user intervention, are labeled automatic. The automatic tests report failures with error messages.

Test 1: Hard Disk (Automatic)

- o Recalibration of hard disk
- o Random seek of hard disk

Test 2: Floppy Disk (Interactive)

- o Formats the floppy disk
- o Random seek of floppy disk

Test 3: Keyboard (Interactive)

- o Determines whether the keyboard and mouse work properly

Test 4: Video (Interactive)

- o Tests all screen parameters

Test 5: Memory & Parity (Interactive)

- o Performs data test
- o Performs address test
- o Performs random pattern test

Diagnostics

Test 6: Communications (RS232 Ports) (Automatic)

- o Self-test of the RS232 Expansion Ports
- o Transfer test at 300 Baud through 19200 Baud

Test 7: Modem (Automatic)

- o Internal loopback sequence test used to check:
 - 1200 or 300 Baud
 - no parity, odd parity or even parity
 - 7-bit or 8-bit characters

Test 8: Dialer (Interactive)

- o Tests touch tone pulses
- o Tests rotary dial pulses

Test 9: Processor (Automatic)

- o Map RAM test:
 - Data
 - Address
 - Random pattern
- o Parity test:
 - Read/write
 - Execution test
- o Map translation test:
 - Subtest 1
 - Subtest 2
- o Page fault test
- o User I/O interrupt test:
 - Subtest 1
 - Subtest 2
- o Clock test
- o Page protection test

Test 10: Parallel Printer (Automatic)

- o Subtest 1 (status test)
- o Subtest 2 (transfer test)

Test 11: Real Time Clock (Interactive)

- o Read Write test
- o Operation test

Test 12: Return to Main Menu

- o Returns you to the main menu diagnostics

Diagnostic Test Descriptions

The following descriptions include test algorithms, error messages, and screen displays for the floppy disk diagnostic tests.

Memory Test

This test has three subtests: data, address, and random pattern. The same algorithm is used to test map RAM, dynamic RAM, and video memory.

Memory Subtest: Data Test

This test writes a walking ones pattern to a memory location and then reads it back. It tests all memory locations. If the data read back is incorrect, it reports the address, data written, and data read back in the following error message:

Memory error at Addressw X; Wrote X; Read Back X

Memory Subtest: Address Test

The address test has the following three-step algorithm for each address tested:

- o Writes data to a memory location.
- o Reverses one bit in the address and writes different data.
- o Checks the first address to see if there is a change. If data changes, the test generates an error message reporting the address line that has changed and the memory bank being tested. For example, it writes AAAA to addresss 000000 and then writes 5555 to address 000001. It then reads the contents of address 000000. If the contents are not still AAAA, address line A0 is bad. The following error message appears:

Memory error: Connection on address line X is bad at Bank X

Diagnostics

Memory Subtest: Random Pattern Test

During this test, a random number generator sequence generates a 64KB random pattern of 16-bit words. This pattern is then written to memory, repeating every 64KB. Then the random number generator is invoked again, and the pattern is read back from memory and compared with the function generator output.

Memory Test Error Message

If the two patterns differ, the address data written and data read are displayed in the following error message:

Memory error at Address X; Wrote X; Read Back X

Memory Test Screen Display

MEMORY TEST

DATA TEST

Memory test will begin at 2F000, end at 7FFFF

Testing.....

ADDRESS TEST

Memory test will begin at 2F000, end at 7FFFF

RANDOM PATTERN TEST

Memory test will begin at 2F000, end at 7FFFF

EXPANSION MEMORY TEST

Note

The preceding message is displayed if expansion memory is not present. If it is present, the preceding memory tests are repeated on expansion memory.

Parity Test

This test forces bad parity on each location and checks for an error during each memory access.

It first writes 8000 to address E40000 to set EE+ high at IC7K (pin 4) high. Next it writes 8000 to address E41000 to set PIE+ high (IC7K, pin 5). Then memory is written to and read to see if an interrupt results. If a parity error does occur, the following message appears:

Unexpected parity error at location X

Then the BP+ at IC7K (pin 6) is set low by writing 0 to address E42000. This causes bad parity to be written during any access to memory. Next, a selected memory location is written. Then that location is read. A level 7 interrupt results during the read. This interrupt causes the current address and data to be stored in bus status registers BS0 at address 430000 and BS1 at 440000 and the error bit status to be stored in the general status register at 410000.

Parity Test Error Messages

If the interrupt does not occur, the following messages appear:

No Parity Interrupt at location X
BSR incorrect after parity error at location X
BSR0 = X, BSR1 = X

Parity Test Screen Display

Parity Test

PARITY TEST - READ/WRITE TEST
Memory test will begin at 2F000, end at 7FFFF
Reached Address 30000
Reached Address 40000
Reached Address 50000
Reached Address 60000
Reached Address 70000
PARITY TEST - SUBTEST 2 EXECUTION TEST

Map Translation Test

This test performs the following steps:

- o Initializes all pages to one-to-one correspondence between logical and physical address space.
- o Checks status bits of map registers. First it writes page present to all addresses and then reads them all. The status bits should show all pages present and read. Next it writes to every location in memory and checks to see that every page shows that it has been written to.
- o Interchanges physical and logical page addresses and verifies that content has been interchanged.

Diagnostics

The map translation test checks the status bits and page table entry swapping. The subtests are:

- o Read/write memory test (checks access and dirty bits)
- o Map test (checks page table entry swapping)

Subtest 1 (read/write memory test) performs the following steps:

- o Sets status register of a page to valid (01)
- o Reads from a memory location on that page
- o Reads the status of the page and verifies that it has changed to read (10)
- o Writes to a memory location on that page
- o Reads the status of the page and verifies that it has changed to written to (11).

Subtest 2 checks mapping to the correct physical memory location as follows:

- o Writes to two locations on different pages.
- o Swaps the page table entries for the two pages.
- o Reads back the two locations and verifies that the values are swapped.

Map Translation Test Error Messages

Subtest 1 can return the following error messages:

Page access bit not set for page number
Page access bits wrong: page number and page bits are X
Page mapping error
Page dirty bit not set for page number

Map Translation Test Screen Display

MAP TRANSLATION TEST
MAP TRANSLATION SUBTEST 1
MAP TRANSLATION SUBTEST 2

Page Protection Test

The page protection test has the following three parts:

- o CPU page fault

During this portion of the test, a page is declared not present and the processor generates bus errors by reading and writing to it.

The following error messages may occur during this test:

No page fault received on write
Map add = X, Map = X, Mem add = X

No page fault received on read
Map add = X, Map = X, Mem add = X

Bus Error when none expected
Map add = X, Map = X, Mem add = X

- o Writing to page, not write-enabled, by user

This portion of the test sets the processor to user mode and writes to a memory page that is write-disabled. It accesses the first location of every page except those used by diagnostics.

The following error messages may occur during this test:

No Bus Error received on write, after page write being disabled
Map add = X, Map = X, Mem add = X

- o Access below 512 KB by user

This portion of the test sets the 68010 to user mode and writes to every location below 512 KB except that contained by diagnostics. It verifies BSR0 for MMU, BSR0 and BSR1 for faulted address, and RAM for write disabled.

The following error messages may occur during this test:

No Bus error detected, while user accessing below 512k memory
Disabled Ram writing failed at mem loca X

BSR incorrect after Bus error at location X
BSR0 = , BSR1 =

Diagnostics

Page Protection Test Screen Display

PAGE PROTECTION TEST

Format Disk Test

This test has the following three parts:

- o Reads volume home block (VHB) and bad block table (BBT)

This portion of the test reads the VHB and BBT and calculates a check sum. If the check sum is correct, it saves the VHB and BBT to rewrite them later. If the check sum is incorrect or the VHB is not present, new VHB and BBT are written after formatting is complete. Whether check sum is correct or not, it continues formatting.

- o Formats all sectors

This portion of the test formats the disk one track at a time. After each track is formatted, it reads the status register to see if an error has occurred.

If the status register reports an error, the following message appears:

Error during Disk Format: Response = XX

(XX is the hexadecimal contents of the status register.)

After the disk is formatted, the VHB and BBT are written and read back and a check sum is calculated. If the check sum is incorrect, the following message appears:

VHB write failed. Disk needs to be re-initialized

If the BBT check sum is bad, the following message appears:

Bad block table write failed. Disk needs to be re-initialized

Format Disk Test Screen Display

FORMAT DISK
Formatting cylinder xx

Recalibration Test

This test has the following three parts:

- o Seeks to track 0
- o Reads status register for error

If an error is present, the following message appears:

Can't Recal: Response = XX

- o Reads VHB and BBT and calculates the check sum

If the check sum is incorrect, the following error message appears:

Recal Failed

Recalibration Test Screen Display

Recal Disk

Surface Test

This test writes 6DB6DB6D to all byte locations in one track, 16 sectors. While writing this pattern, it checks the status register for errors.

If an error occurs, the test determines the number of the sector that has the error by writing 6DB6DB6D to one sector at a time. After each sector is written, the status register is checked. When the error is found, the BBT is updated with the number of the sector that generated the error.

If no errors are generated while the track is being written, the test reads the contents of all 16 sectors and checks the data for any errors.

If an error is found, it reads the sectors one at a time to determine the one containing the error and updates the BBT. If no error is found, it checks the next track.

If all tracks are written without error, the test reads all tracks one at a time and checks for error. If an error occurs, it reads each sector to find the one that contains the error and adds it to the BBT.

Diagnostics

Surface Test Error Messages

Can't Write the new VHB: Response = XX
Can't Write the new Bad Block Table: Response = XX
Error on Write: Response = XX, Start Block = XX
Error on Re-Read: Response = XX, Start Block = XX
Re-Read Data Fail: Start Block = XX, Byte = XX,
 Received XX, Expected XX
Error on Check-Read: Response = XX, Start Block = XX
Check-Read Data Fail: Response = XX, Start Block = XX
Initiating Check Read for pass XX
Bad Block Table Overflow when adding Sector XX
Bad Block Table: Multiple use of alternate XX

Surface Test Screen Display

 Surface test
Volume Name: FLOPPY
Pass 1
Testing blocks xxx...yyy

User I/O Interrupt Test

This test tries to create a bus fault by having a user program attempt to access a register outside its space. If this does not cause a bus fault, the following error message appears:

 No bus error when user access I/O address X

User I/O Interrupt Test Screen Display

 USER I/O INTERRUPT TEST
 USER I/O INTERRUPT SUBTEST 1
 USER I/O INTERRUPT SUBTEST 2

Clock Test

This test sets up a clock interrupt so that a digit appears on the screen every second and counts down from 9. The screen shows 9, 8, 7, 6, ..., 1.

The following error message may appear during the clock test:

 Time out while waiting for 60 Hz interrupt

Clock Test Screen Display

CLOCK TEST

Subtest 1 - Timer 1/Counter 2 TEST

9 8 7 6 5 4 3 2 1 0

Printer Test

The printer test has two parts. First the status register is read, and then a barber pole printing pattern is sent to the printer.

Printer Test Screen Display

LINE PRINTER TEST

LINE PRINTER SUBTEST 1, Status test

Line printer is selected.

LINE PRINTER SUBTEST 2, Transfer test

Line printer is selected.

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Communications Test

This test does a loopback test and checks combinations of different baud rates, number of bits, and types of parity as listed below:

- o Baud rate is 300, 1200, 2400, 4800, 9600, or 19,200
- o Bit count is 5, 6, 7, or 8
- o Parity is none, odd, or even

Communications Test Error Messages

Overflow error

Framing error

Parity and framing error

Diagnostics

Communications Test Screen Display

COMMUNICATION TEST (Self-test & Transfer test)

SELF-TEST

TRANSFER TEST

300 Baud

7 bits/character	no parity
7 bits/character	odd parity
7 bits/character	even parity
8 bits/character	no parity

1200 Baud

7 bits/character	no parity
7 bits/character	odd parity
7 bits/character	even parity
8 bits/character	no parity

2400 Baud

7 bits/character	no parity
7 bits/character	odd parity
7 bits/character	even parity
8 bits/character	no parity

4800 Baud

7 bits/character	no parity
7 bits/character	odd parity
7 bits/character	even parity
8 bits/character	no parity

9600 Baud

7 bits/character	no parity
7 bits/character	odd parity
7 bits/character	even parity
8 bits/character	no parity

19200 Baud

7 bits/character	no parity
7 bits/character	odd parity
7 bits/character	even parity
8 bits/character	no parity

After 19,200 baud, the program returns to the main diagnostics menu.

Modem Test

During this test, an internal loopback test sequence checks all possible combinations of the following parameters:

- o 300 or 1200 baud
- o 7- or 8-bit characters
- o No parity, odd parity, or even parity

Modem Test Error Messages

SELF TEST failure detected
MODEM TRANSFER TEST, receive error - parity error,
expected XX

Modem Test Screen Display

MODEM TEST (Self-test & Transfer test)
SELF-TEST(B212 mode) at 300 baud..
Test passed with no error detected.
SELF-TEST (B212 mode) at 1200 baud..
Test passed with no error detected.

DATA TRANSFER TEST at 300 baud..

7 bits/character no parity

7 bits/character odd parity

7 bits/character even parity

8 bits/character no parity

Diagnostics

8 bits/character

odd parity

```
*****
*****
*****
*****
```

8 bits/character

even parity

```
*****
*****
*****
*****
```

Test passed with no error detected.

DATA TRANSFER TEST at 1200 baud

7 bits/character

no parity

```
*****
*****
*****
*****
```

7 bits/character

odd parity

```
*****
*****
*****
*****
```

7 bits/character

even parity

```
*****
*****
*****
*****
```

8 bits/character

no parity

```
*****
*****
*****
*****
```

8 bits/character

odd parity

```
*****
*****
*****
*****
```

```
8 bits/character          even parity
***** *****
***** *****
***** *****
***** *****
```

Test passed with no error detected.

Dialer Test

This interactive test generates either touch tones or rotary dial pulses.

Connect outside phone lines. Each number is dialed as you enter it, and you can hear it on the speaker. To connect the handset to the phone line when answering a call, type c after the dialed number answers. To disconnect, type q.

Note

You must have the handset offhook before you type c. You then type h to put the line on hold.

Select Test 10 from the floppy disk main diagnostics menu. The following screen appears (DTMF means dual-tone multifrequency):

```
-- INTERACTIVE DTMF TEST --
Select line 1 or line 2 for testing:
```

When you select a line, the following message appears:

Enter digit 0-9;*,# for dialing. To connect the hand set for conversation, enter C/c. To toggle line between hold and active, enter H/h. To quit enter Q/q:

When you select a line and enter a number, you hear the touch tones as the number is transmitted, and the number is displayed on the screen. If you enter a series of numbers faster than they can be transmitted, they are stored and transmitted.

When you type q, the preceding message returns. When you select a line and enter numbers for the second time, dial pulses are generated.

Diagnostics

Note

Pulse dialing may not work on certain internal electronic telephone systems.

When you type **q** the second time, the following message appears:

-- **AUTO ANSWER** --

Waiting for incoming call! type **Reset/Break** to exit!

At this point, dial the number of the phone that is connected to your **UNIX PC** from another phone.

Video Test

This interactive test displays the following menu of test patterns:

VIDEO TEST

- 0) All black
- 1) All white
- 2) Half tone
- 3) Vertical bars
- 4) Horizontal bars
- 5) Mosquito net
- 6) Black pattern
- 7) White pattern
- 8) All m's
- 9) Exit

At the end of a test, press any key to get back to this menu.

Please select test number 0 - 9 : (Return is 0)

Screen Descriptions

Test 0 makes the screen solid black.
Test 1 makes the screen solid light.
Test 2 displays a fine dot pattern.
Test 3 displays a sequence of vertical bars.
Test 4 displays a sequence of horizontal bars.
Test 5 displays a combination of Tests 4 and 5.
Test 6 displays a cross for checking screen alignment.
Test 7 is the same as Test 7 with inverse video.
Test 8 fills the screen with the letter m.

Trap Errors

Trap errors are general errors that can occur during any test.

Type = XX, GSR = XX, BSRO = XX, BSR1 = XX

Repeated fault

Bad GSR after page fault

Bad GSR after execution Page fault

BSR not correctly set after Page Fault

BSR0 = XX, should be XX BSR1 = , should be XX

Unexpected bus error, GSR = XX, PC = XX, RPS = X

Unexpected NMI, PC = XX, RPS = XX

GSR = XX BSRO = XX BSR1 = XX

Unexpected interrupt from level XX

PC = XX RPS = XX GSR = BSRO = XX BSR1 = XX

HD or DMA interrupt from level XX, PC = XX, RPS = XX

GSR = XX BSRO = X BSR1 = XX

XX Interrupt level XX, PC = XX, RPS = XX

User I/O flag in GSR not set during User I/O test

LWT in GSR set during User I/O fault

Bus Grant set to DMA cycle during User I/O fault

BSR not correctly set after User I/O fault

BSR0 = XX, should be XX BSR1 = XX, should be XX

Expert Mode Diagnostics Program

The expert mode diagnostics program contains more subtests than are available from the floppy disk diagnostics main menu. In addition, it allows selection of specific subtests without running the complete test.

To enter expert mode diagnostics, type `s4test` and press <Return> instead of selecting a test number from the floppy disk main diagnostics menu. To exit from expert mode diagnostics, type: `u` and press <Return>.

Diagnostics

A `command>` prompt is displayed to show that expert mode diagnostics has been entered.

To see a menu of expert mode diagnostics, type `?` and press `<Return>`. The following menu scrolls on the screen:

Commands formatted at follows:

```
[<repeat-count>]<command-letter>[L | C]      or
[<repeat-count>]:<test-number>[, <subtest-number>][L | C]
    P[E | M] toggles Parity Enable | Page Mode
    LE toggles Parallel Printer Echo Mode
    V for Diagnostic Version,      U to return to User Menu
    Multiple commands may be separated by ;
```

Command	Description
1	Full System test.
2	Initialize Hard disk.
3	Enter Bad blocks.
4	Park Disk Heads.
7	Reboot System.
11	Hard Disk test.
12	Floppy Disk test.
13	Key board & Mouse Test.
14	Video test.
15	Memory & Parity test.
16	Communication test.
17	Modem Test.
18	Dialer test.
19	Processor test.
20	Parallel Printer test.
21	Real time clock test.
31	Interactive device test.

Note that entering page mode prevents the top items from rapidly scrolling off the screen. To enter page mode, type PM and press <Return> before typing ?. Press <Page> to see the next page of the menu. Type PM and press <Return> again to exit page mode.

Disk Drive Commands

When the **command>** prompt appears, type **i** (Initialize command) and press <Return>. The **disk>** prompt appears. To return to the **command>** prompt, type **q**.

To select the drive that you want to test, type **dr n**, where **n** is either 0 (default) for the floppy disk or 1 for the hard disk. Then issue the Initialize (**i**) command or manually turn on the motor, select the drive, and reset the drive.

To include more than one test in a single command, use semicolons. For example:

```
disk> step 10; rd 1; sb; step - 10; rd 1
```

To repeat a command, type **; r** at the end of the command. To terminate the repeat option, press any key.

Read and Write Commands

Table 3-1 Read/Write Command Format

Command	Short Form	Syntax	Comment
Read	rd	rd [[sector] sector]	
Write	wr	wr [[sector] sector]	
Read ID	ri	ri	FD only
Read Track	rt	rt	FD only
Write Track	wt	wt	FD only

All Read and Write commands operate on the specified sector(s) on the current track. To read from another track, first execute a Seek or a Step command.

The Read and Write commands use the sector buffer.

The Read ID command uses the ID buffer.

The Read Track and Write Track commands use the track buffer.

Diagnostics

Seek and Step Commands

Table 3-2 Seek and Step Command Format

Command	Short Form	Syntax	Comment
Restore Recal Home Seek Step	rs rc h s (none)	rs rc h s track step number	FD only

Restore and Seek commands read the ID field at the destination track. The Step command issues step pulses without verifying.

Register Commands

Table 3-3 Register Command Format

Command	Short Form	Syntax	Comment
Register	rg	rg	
Status	st	st [number]	
Command			
Register	cr	cr [number]	
Track			
Register	tr	tr [number]	FD only
Sector			
Register	sr	sr [number]	FD only
Data			
Register	dr	dr [number]	FD only
Sector Count			
Register	sc	sc [number]	HD only
Sector Number			
Register	sn	sn [number]	HD only
Cylinder Low			
Register	cl	cl [number]	HD only
Cylinder High			
Register	ch	ch [number]	HD only
Size Drive Head			
Register	sdh	sdh [number]	HD only

Register commands with no argument show the register. Register commands with an argument write to the register.

Buffer Commands

Table 3-4 Buffer Command Format

Command	Short Form	Syntax
Sector Buffer	sb	sb [number]
Track Buffer	tb	tb [number]
ID Buffer	ib	ib [number]

Buffer commands with no arguments show the buffer. Buffer commands with an argument fill the whole buffer with that number. The sector buffer holds 512 bytes, the ID buffer holds 6 bytes, and the track buffer holds approximately 8 KB.

Miscellaneous Commands

Table 3-5 Miscellaneous Command Format

Command	Short Form	Syntax	Comment
Drive	dr	dr [number]	
Initialize	i	i	
Mtron	(none)	mtron	FD only
Mtroff	(none)	mtroff	FD only
Format	fm	fm track	
Force			
Interrupt	fi	fi	FD only
Help ?	?		
Radix	(none)	radix [number]	
Quit	q	q	
Head	hd	hd [number]	
Reset	(none)	reset	
Repeat	r	r	

Diagnostics

The Mtron (motor on) and Mtroff (motor off) commands control the floppy motor.

The Head command selects a head for further operations.

The Format and Radix commands do not work.

Reading/Writing to Hard Disk with Expert Mode

Use the following sequence of commands and prompts to read and write data to a sector of the hard disk drive using expert mode diagnostics.

- 1 Load floppy disk diagnostics.
- 2 When the test select prompt below the main diagnostics menu appears, type s4test and press <Return>.

The command> prompt appears.

- 3 Type 1 (the Initialize command) and press <Return>.

The disk> prompt appears.

- 4 Type dr 1 and press <Return> to select the hard disk.

The disk> prompt reappears.

- 5 Type 1 and press <Return> to initialize the drive.

The LED on the drive lights up.

From this point, use the Sector Buffer (sb), Read Sector (rd), and Write Sector (wr) commands to fill the sector buffer with data, write the contents of the sector buffer to a sector, read the sector into the buffer, and then read the sector buffer contents.

For example, to fill sector 0 with 5555s and then read it back, issue the following sequence of commands after the disk> prompt:

- 1 Type sb to read the sector buffer.

The current contents of the sector buffer appear.

- 2 Type sb 5555 to fill the sector buffer with 5555's.

- 3 Type sb to verify that the sector buffer contains 5555's.

- 4 Type wr 0 to write the contents of the buffer to sector 0.

-
- 5 Type **sb 0** to fill the sector buffer with 0s, so you can see that the buffer contents have changed when you read sector 0 from the drive into the buffer.
 - 6 Type **sb** to verify that the sector buffer contains all 0's.
 - 7 Type **rd 0** to read from sector 0 and put the contents into the sector buffer.
 - 8 Type **sb** to read the sector buffer, which now shows 5555's.

4 Logic Board Test Procedures

This section is a collection of test procedures for component-level troubleshooting of the UNIX PC logic board. In addition to standard test equipment, the following items are required:

- o A set of debugger EPROM's
- o A set of map RAM test EPROM's
- o A set of RAM test EPROM's
- o A set of silent loader EPROM's
- o A logic analyzer
- o An unintelligent terminal
- o An EPROM programmer
- o A master set of PAL's
- o A PAL programmer
- o A supply of the three semicustom gate arrays

The following reference books will also be useful:

- o Motorola's MC68010 16-Bit Virtual Memory Microprocessor
- o Motorola's MC68000 Programmer's Reference Manual
- o Western Digital's Storage Management Products Handbook
- o Intel's Microprocessor and Peripheral Handbook

Information provided with the board usually indicates to an experienced technician the tests that should be used. If the nature of the problem is not known, however, the first step in troubleshooting is to determine the highest level of diagnostics that will run. The higher the level, the larger the portion of the board that must be working and thus can be ruled out as the cause of the problem. Procedures associated with that level are then used to pinpoint the cause of the problem. (Some of these procedures have training value as well as testing value, so it is recommended that they be practiced on a known good board.)

The diagnostic levels are listed below in ascending order:

- o Map RAM EPROM
- o RAM EPROM
- o Silent loader
- o Debugger program
- o Floppy disk diagnostics

Logic Board Test Procedures

Map RAM EPROM Program

The map RAM EPROM program executes the following tasks:

- o Performs data test
- o Performs address test

Data Test

The map RAM EPROM tests the map RAMs and outputs data to the LEDs as listed in Table 4-1, (LED 4 is the one nearest the corner of the board) :

Table 4-1 Logic Board LED STATES

Function	LED 4	LED 3	LED 2	LED 1
Testing data	On	Off	Off	Off
Testing address	On	On	Off	Off
Data error	On	Off	Off	On
Address error	Off	On	On	Off

If a data error pattern appears, the EPROM is executing a loop that continuously reads and writes to an address where the data read back differs from the data written. This memory cycle may be observed using a logic analyzer. Set the analyzer to trace from the beginning of this loop. In the EPROM currently being used, this loop is located at 80007A hexadecimal, the address of the first instruction in the loop. The loop contains the following assembly instructions:

```
1$  MOVEW    D1,A0@  
      MOVEW    A0@,D0  
JMP  1$
```

The MOVEW instruction moves a 16-bit word from internal 68010 register D1 to the memory location whose address is contained in 68010 address register A0. Thus the first instruction is a memory write instruction. The second instruction is similar except that it reads from memory to register D0. The third instruction is a jump that causes the first instruction to repeat. Thus, once this loop is entered, these instructions will repeat as long as the power is on.

When the logic analyzer is set to trace starting at the location of the first instruction, it shows the address and data that were written during the first instruction and read during the second. The data read must differ from the data written for the program to have entered the loop. An example of address and data follows:

Address	Data	Type of Cycle
400000	0000	Data write
400000	0800	Data read

In this example, data bit D11 is a 0 during a write and a 1 during a read. Because each RAM chip contributes a single bit to the data bus, this indicates that the problem is caused by one of the four RAM chips that output data bit D11. There is one chip for each of the rows w, x, y, and z. Address bits A1 and A2 select the row; both are 0 in this example, so the chip in row w is indicated.

Address Test

In the address test, the program first writes various data to all memory locations. It then checks all memory to see if there are any locations that do not have proper data. If an address line is faulty, shorted, open, or has some other problem, the program assumes that, at some point in the process of writing to all locations, a write in some location (call it new) changes the contents of a previous location (call it old). When it reads all locations and finds one that is incorrect, the program considers this location to be old. The old location is stored.

The next phase of the test determines the new location. To do this, the program starts a second writing operation to all memory locations. Each time it does a write, the program checks the old location to see if the contents have changed. When the program detects a change in the contents of the old address, it stores the address written to, because this must be new.

Logic Board Test Procedures

Error Loops

The following tables show the addresses of machine code that executes when the map RAM EPROM program finds an address or data error. These serve as trace addresses when a logic analyzer is used to determine the error addresses and data.

Data error (LEDs 1 and 4 on; LEDs 2 and 3 off):

Address	Register Notation	Description
800084:	MOVW D1, (A0)	Writes contents of D1 to address in A0
800086:	MOVW (A0), D0	Reads contents of address in A0
800088:	JMP 800084	Returns to top of loop

Both error addresses found (LEDs 4, 3, and 2 on; LED 1 off):

Address	Register Notation	Description
8000EA:	MOVW (A4), D0	Reads memory address in A4
8000EC:	MOVW D3, (A4)	Writes to memory; A4 holds address that causes contents of memory address in A0 to change when it is written to
8000EE:	MOVW (A0), D0	Reads memory address in A0
800100:	MOVW D7, (A0)	Writes to address in A0
800102:	JMP 8000EA	Returns to top of loop

Second error address not found (LED's 4, 3, 2 on; LED 1 off):

If an address error occurs but the program cannot find the second error address, the following instruction loop is entered:

```
800110:  MOVW (A0), A0
800112:  JMP 800110
```

RAM EPROM Program

The RAM EPROM program executes the following tasks after setting unity map:

- o Performs data test
- o Performs address test

Data Test

The program performs a walking ones and walking zeros test of 512KB of memory. Each address is written to and then the contents are read back. If the contents read differ from those written, the program jumps to the data error loop.

Address Test

The address test of RAM is similar to the test of map RAM above except that several different data patterns are written. First a data pattern of 0-256 is written to all memory addresses. Then memory is divided into eight 64K blocks. Each block is then tested by dividing it into 256 subblocks of 256 bytes each and writing a different data word to each subblock. As in the map RAM address test, there are two error loops, one when both error addresses have been found and one when the second address cannot be found.

Error Loops

The following addresses are for machine code that executes when the RAM EPROM program finds an address or data error. These serve as trace addresses when a logic analyzer is used to determine the error addresses and data.

Logic Board Test Procedures

Data error loop (LED's 1 and 4 on; LED's 2 and 3 off):

```
8000A4:  MOVW D1, (A0)
8000A6:  MOVW (A0), D0
8000A8:  JMP 8000A4
```

Both error addresses found (LED's 4, 3, 2 on; LED 1 off):

```
8001EE:  MOVB (A4), D0
8001F0:  MOVB D3, (A4)
8001F2:  MOVB (A1), D0
8001F4:  MOVB D7, (A1)
8001F6:  BRA 8001EE
```

Second error address not found (LED's 4, 3, 2 on; LED 1 off):

```
800202:  MOVB (A1), D0
800204:  BRAL 800202
```

Debugger Program

The debugger is a breakpoint monitor program. With the debugger, the user can modify memory and run programs. That is, the user can enter and run programs, disassemble instructions, and set breakpoints. The debugger includes a load command that allows downloading diagnostics into memory from another computer. This can be used to load diagnostics from a machine that can load diagnostics from a floppy into one that cannot.

To set up the debugger program:

- 1 Replace the boot ROM's with the debugger ROM's.
- 2 Connect the **UNIX** PC to an unintelligent terminal via the RS-232-C port.
- 3 Push the Reset button.

The following message appears:

```

S4      MC68010      ROM      DEBUGGER      V1.0

COPYRIGHT 1984 BY CONVERGENT TECHNOLOGIES INC.

SR=XXXXXXXX PC=00800F66 SP=00800F66 UP=XXXXXXXX
D0=XXXXXXXX D1=XXXXXXXX D2=XXXXXXXX D3=XXXXXXXX
D4=XXXXXXXX D5=XXXXXXXX D6=XXXXXXXX D7=XXXXXXXX
A0=XXXXXXXX A1=XXXXXXXX A2=XXXXXXXX A3=XXXXXXXX
A4=XXXXXXXX A5=XXXXXXXX A6=XXXXXXXX A7=XXXXXXXX
00800F66      bras    0x00800F64
DBG>
    
```

The program counter (PC) shows the address of the next instruction to be executed. SP and UP are supervisory and user stack pointers, respectively, D0-D7 are data registers, A0-A7 are address registers, and SR is the status register.

After the debugger (DBG>) prompt, type **he** (for the Help command). The following message appears, listing the debugger program commands:

```

COMMANDS:  BR, BC, BO, DB, DE, DI, DM, DR, DW, GO, HE, LO,
           MB, MM, MR, MW, WM, WW, WB, TR
    
```

These commands are entered after the DBG> prompt is displayed. The first group, the breakpoint group, consists of BR and BC. BR followed by an address sets a breakpoint at that address; BC followed by an address clears the breakpoint at that address.

For example, to set and clear a breakpoint at address 40000:

1 After the DBG> prompt, type **br 40000** and press <Return>.

The following message appears:

```

1 BREAKPOINTS SET AT:  00040000
    
```

2 Type **bc 40000** and press <Return> to clear the breakpoint.

Logic Board Test Procedures

Using the debugger ROM's, you can set and clear as many breakpoints as necessary depending on your application. If you try to clear a breakpoint at an address where one does not exist, the following message appears:

NO BPT AT THAT ADDR

When a program containing several breakpoints stops at any given breakpoint, type go and press <Return> after the DBG> prompt to continue program execution to the next breakpoint.

The next group of commands, the display group, includes DB, DF, DM, DR, and DW. When followed by an address, command DB (display byte) causes the next 16 bytes of data to be displayed. Pressing <Return> causes 16 more bytes of data to be displayed; typing / and pressing <Return> recalls the DBG> prompt.

For example, to display 16 bytes starting at address 40000:

- 1 After the DBG> prompt, type db 40000 and press <Return>.

The following message appears, displaying the 16 bytes:

00040000: XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX

- 2 Press <Return> again.

The screen displays the next 16 bytes:

00040010: XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX

- 3 Type / and press <Return> to recall the DBG> prompt.

The DF (display all registers) command presents all registers internal to the 68010. To use this command, simply type df and press <Return> to display all registers.

The DM (display 32-bit word) command, when followed by an address, displays the 32-bit word starting at that address. Pressing <Return> gives the next 32-bit word; typing / and pressing <Return> recalls the DBG> prompt.

The DR (display register) command displays each of the 68010 registers just as the DF command does.

The DW (display 16-bit word) command, when followed by an address, displays the 16-bit word located there. Pressing <Return> gives the next 16-bit word; typing / and pressing <Return> recalls the DBG> prompt.

The B0 (boot the UNIX PC) command first checks to see if there is a bootable floppy inserted. If not, it boots from the hard disk.

The G0 command, when followed by an address, causes program execution to begin at that address.

HE is the Help command, which has already been discussed.

L0, the Load command, downloads a program into memory from the RS-232-C port.

The next group of debugger commands, the modification group, includes MB, MM, MR, and MW. With this group, the user can inspect and change the contents of various addresses and registers in the UNIX PC.

The MB (modify byte) command, when followed by an address, displays the 16-bit word at that address and enables the user to modify the word. The least significant bit of the address indicates whether the upper or lower half of the 16-bit word can be modified. If it is clear (0), the upper half of the 16-bit word can be modified; if it is set (1), the lower half can be modified. Pressing <Return> allows the next byte to be modified; typing / and pressing <Return> recalls the DBG> prompt.

The MM (modify 32-bit word) command enables the user to modify an entire 32-bit word at a specified address. Pressing <Return> allows the next 32-bit word to be modified; typing / and pressing <Return> recalls the DBG> prompt.

The MR (modify register) command displays each of the 68010 registers so the user can find the one that needs to be modified. It then allows the user to modify that register. Pressing <Return> displays the next register; typing / and pressing <Return> recalls the DBG> prompt.

The MW (modify word) command lets the user modify the 16-bit word at the specified address. Pressing <Return> gives the next word; typing / and pressing <Return> recalls the DBG> prompt.

The write commands, including WM, WW, and WB, enable the user to change the contents of various addresses just as the modify commands do, but the write commands do not display the previous contents. Pressing <Return> lets you write to the next address; typing / and pressing <Return> recalls the DBG> prompt.

The TR (trace trap) command allows single-step execution through the user program. TR followed by an address starts the trace at that address.

Logic Board Test Procedures

Shadow Addresses

Address bits A20 and A21 are not decoded when RAM is addressed. The result is that each RAM address has three shadow addresses. When you write data to an address that has a shadow, the data appears in the shadow. For example, 08000h is the shadow of 000000h, and any data written to 000000h appears in 080000h.

The shadows for the lowest and highest RAM addresses are:

Address	Shadow Address
000000h (lowest)	080000h 100000h 180000h
07ffffe (highest)	0ffffeh 17ffffeh 1ffffeh

Machine Language Programming

Table 4-2 on the next page, contains a few instructions for writing short programs, which can be loaded and run using the debugger program.

Definitions

D_n and A_n refer to address and data registers inside the 68010, where n is any number from 0 through 7. (A_n) refers to the contents of memory pointed to by the address in address register A_n.

Instructions consist of one op code word followed by extension words, if used.

2A_n in the op code instruction means 2 times the number of the address register. For example, to use the move instruction below (3/2A_n/8/D_n) to write the contents of data register D2 to the memory location contained in address register A1, the op code is 3282.

Table 4-2 Program Instructions

Machine Code	Register Notation	Description
3/2An/8/Dn	MOVE Dn to (An)	Writes contents of data register Dn to memory location contained in An.
3/2Dn/3/C [ext. word]	MOVE #word to Dn	Loads extension word into data register Dn.
2/2An/7/C [00XX]	MOVEA <ea>, An	Moves the two extension words into address register An. The first extension word contains the most significant address digits.
5/3/4/Dn	Dn = Dn - 1	Subtract Quick. Decrements data register Dn.
B/2Dn/7/C [immed. data]	CMP <ea>, Dn	Compares immediate data to Dn. Subtracts source operand from specified data register and sets condition codes according to the result; the data register is not changed.
6/6/X/X	BNE <label>	Branch not equal. If this instruction is preceded by a CMP instruction (above) and the data words compared are not equal, then program execution continues at a location obtained by adding the displacement represented by <label> and the address of the next instruction. The displacement is a 2's complement form.
6/0/X/X	BRA <label>	Program execution continues at the address of the next instruction plus the displacement. The displacement is a 2's complement form.

Logic Board Test Procedures

To calculate the 2's complement displacement for a BNE or BRA instruction (see preceding table):

- 1 Count the number of bytes back to the first instruction in instruction.
- 2 Convert this number to 2's complement by:
 - o Writing it as an 8-bit binary number
 - o Changing each 0 to 1 (binary 1's complement)
 - o Adding 1 (binary 2's complement)
 - o Converting to hexadecimal

Walking Ones Test Program

The following program sets a pattern of walking ones in the first 1/2KB of memory:

```
070000: 303C    MOVE 1h to D0
070002: 0001

070004: 307C    MOVEA 0100h to A0
070006: 0100

070008: 3100    MOVE D0, -(A0) (loop)

07000A: E358    ROL D0

07000C: B0FC    CMPA (compare A0 with 0)
07000E: 0000

070010: 66F6    BNE (branch if not equal to loop)

070012: 4EF9    JMP (return to debugger)
070014: 0080
070016: 0EE0
```

Read/Write Loop Program

The use of an oscilloscope in troubleshooting the logic board is limited because most signals, such as address and data, do not have repeating waveforms that an oscilloscope can synchronize on. This problem can be solved with a short machine language program that continuously reads and writes the same address in an endless loop.

The program in Table 4-3 can be loaded into memory using the debugger memory write (MW) command and executed by typing go followed by the starting address of the program. Once the program is executing, an oscilloscope connected to a chip select pin being addressed by the program synchronizes easily because the chip-select pulse repeats about every 2 micro-seconds. A second oscilloscope channel is used to measure logic levels on address and data lines when the chip select is active.

To see how this works, execute the following procedure on a known good logic board. In this example, data 0F00, which turns off the LEDs, is written to address 4A0000.

- 1 Load the program shown below using the MW command.

Register notation and description are given to aid understanding. Enter address and data only.

Table 4-3 Read/Write Loop Program

Machine Code	Register Notation	Description
070200:303C 070202:0F00	MOVE 0F00	Moves 0F00 to data register D0.
070204:207C 070206:004A 070208:0000	MOVEA.1	Loads address register A0. Two most significant address digits 4A. Four least significant address digits 0000.
07020A:3080	MOVE D0 to (A0)	Writes D0 to memory location in A0.
07020C:3210	MOVE (A0) to D1	Reads contents of memory location in A0 and puts it in D1.
07020E:60FA	BRA	Branch always--returns program execution to data write instruction at 07020A.

Logic Board Test Procedures

- 2 Verify correct loading by typing `dl` (the disassemble command) followed by `070200`, the starting address of the program.

The instructions disassemble as shown below. Press <Return> to show the next instruction.

```
070200: #0F00, A0
070204: #004A00, A0
07020A: MOVEW D0, A0@
07020C: MOVEW A0@, D1
07020E: BRA 0x007020A
```

- 3 Run the program by typing `go 070200` <Return>.

The program executes and the `DBG>` prompt disappears from the screen.

- 4 Observe the waveforms by connecting an oscilloscope to IC27B (pin 11).

- 5 Stop program execution by pushing the Reset button.

The `DBG>` prompt reappears.

Note that the starting address to load this program is arbitrary. You can load it anywhere you like in memory without changing the program code. The data word in the instruction at 070202 and the address data in the instruction at 070206 are also arbitrary. The first two digits of the address at 070206 are always set to 0, because it takes two words, or eight hex digits, to load an address that uses only six digits; thus the first two are not used.

Turn On/Turn Off Program

The following program writes data to the same address twice, so that a device can be turned on and then turned off. A delay of 64K machine cycles occurs between turning on and turning off.

```

303C  MOVE # to D0
XXXX  Immediate turn on data

323C  MOVE # to D1
XXXX  Immediate turn off data

343C  MOVE # to D2
XXXX  Immediate delay data

207C  MOVE address to A0
00XX
XXXX

3080  MOVE D0 to (A0)

5342  Decrement D2

B47C  Compare immediate data to D2
XXXX  Immediate data set to 0

66F8  BNE (branch not equal)

3081  MOVE D1 to (A0)

60F2  BRA (branch always)

```

Parity Test Procedure

This procedure verifies the ability of the parity circuits to generate a level 7 interrupt when a memory location containing bad parity is read. In addition, it tests the ability of the bus status registers to store the address at which the error occurred.

Logic Board Test Procedures

First the starting address of the debugger is loaded into the level 7 interrupt vector location so that, when the interrupt occurs, the program returns to the debugger. Then the error enable EE+ and PIE+ bits are set high to enable the circuits that generate the interrupt. Next a program that writes bad parity to address 000000 is loaded and run. Then address 000000 is read, causing the parity error circuit to generate a parity error. The parity error causes the address of the error, 000000, to be stored in the bus status registers and a level 7 interrupt to be generated. The bus status registers are then read to verify that they were loaded properly.

- 1 Set up the interrupt vector by writing the following data to level 7 interrupt vector address locations 00007C and 00007E:

00007C: 0080
00007E: 0EE0

Note

800EE0 is the starting address of the debugger.

- 2 Enable errors and interrupts by writing the following data to enable the EE+ and PIE+ bits:

E40000: 8000 Sets EE+ high; IC7K (pin 4) goes high
E41000: 8000 Sets PIE+ high; IC7K (pin 5) goes high

- 3 Load the following program, which writes bad parity to address 000000 (register notation and comments are included to aid understanding):

070300: 303C MOVE #00008000, D0
070302: 8000

070304: 4241 CLR, D1

070306: 207C MOVEA.1 #00E42000, A0
070308: 00E4
07030A: 2000

Loads address to which bad parity is written in A1:

07030C: 227C MOVEA.1 #000000, A1
07030E: 0000
070310: 0000

Sets BP+ high so that bad parity is written:

```
70312: 3080  MOVE D0, A0@  
(Writes D0 to memory location in A0)
```

Writes to test address to cause parity error:

```
070314: 3280  MOVE D0, A1@
```

Resets BP+ low:

```
070316: 3081  MOVE D1, A0@
```

Jumps back to debugger:

```
070318: 4EF9  JMP 0x0080EE0  
07031A: 0080  Returns to debugger  
07031C: 0EE0
```

- 4 Run the program by typing `go 70300 <Return>`.

The program performs the following steps:

- o Writes 8000 to address E42000, which sets the BP+ bit at IC7K (pin 6) high.
- o Writes to address 000000, which sets bad parity at address 000000.
- o Resets the BP+ bit low so that bad parity is not written to any other address after the program returns to the debugger.
- o Jumps back to the debugger.

The debugger message scrolls back on the screen after the program has run.

- 5 Use the debugger to read address 00000.

This causes the parity error circuit to latch the parity error signal and load the address at which the error occurred into bus status registers 0 and 1. The parity error also produces a level 7 interrupt, which causes the debugger message to scroll on the screen.

Logic Board Test Procedures

- 6 Read BSR0 430000 and BSR1 440000.

These bus status registers contain EC00 and 00000, showing that address 000000 is the address that caused the error.

Note

BSR0's least two significant digits contain the two most significant address digits. BSR1 contains the four least significant address digits.

- 7 Check PERR* bit at IC20E (pin 3), which is latched low.

To repeat the test, press the Reset button to clear the latched bits and repeat the preceding steps, omitting step 3.

Page Status Test

This test verifies proper operation of the map RAM page status bits PS0 and PS1. First the status of page 0 is set to page present, write enabled, not read. Then page 0 is read and the page status checked to see that it has changed from not read to read. Finally, page 0 is written to and the page status is checked to verify that it has changed to written.

- 1 Write A000 to address 400000.

This sets status of page 0.

- 2 Read but do not write to address 0.

- 3 Read address 400000.

It contains C000, which indicates that page 0 has been read.

- 4 Write any data to address 0.

- 5 Read address 400000.

It now contains E000, which means that page 0 is present and written to.

MMUERR* Test

This test procedure checks the memory management unit error (MMUERR*) signal. In summary, it:

- o Declares page 0 not present
- o Sets EE+ high to enable the MMUERR* signal
- o Reads page 0, producing the MMUERR* signal.

To test the MMUERR* signal:

- 1 Connect a oscilloscope to the bus error pin (22) of the 68010.
- 2 Write 400000: 0000.

This sets the status of page 0 to not present.

- 3 Write 8000 to address E40000.

This sets EE+, IC7K (pin 4), high.

- 4 Read page 0 by reading address 000000.

A negative pulse appears on the oscilloscope, indicating that a MMUERR* signal has generated a bus error to the 68010. The debugger program crashes.

The following list summarizes possible page status conditions:

400000: 00000	Page 0 not present
400000: 20000	Page 0 present, not write enabled, not read
400000: A0000	Page 0 present, write enabled, not read
400000: C0000	Page 0 present, write enabled, read
400000: E0000	Page 0 present, written, and read

Logic Board Test Procedures

Dummy DMA Test Procedure

The dummy DMA test procedure confirms that the disk bus interface logic can write to a RAM memory location and change its contents. Using the debugger program, follow these steps:

- 1 Set the contents of memory location 000000 to some arbitrary value--for example, FFFF--by typing `mw0` and pressing <Return>.

The system responds with the following address and its current contents:

000000:4EF9

4EF9 is the current contents of location 0. To change the contents, type FFFF and press <Return>. The system responds with:

000000:FFFF

- 2 Escape from the current location and get back to the `DBG>` prompt by typing a period and pressing <Return>.
- 3 When the `DBG>` prompt appears, write 0 to the following locations (note that, because these are write only registers, they show FFFF each time they are read):

4d0000	Disk DMA address register
4d4000	Disk DMA address register
4a0000	Miscellaneous control register

- 4 Write 0 to location 460000, the DMA count register (it shows C000); then write 8001 to it (it shows C001).

You have toggled the least significant bit.

- 5 Examine location 0; it will now be different.

If dummy DMA fails, check the following three signal groups:

- o IDMAR/W, DCNTCS, DCNTWR
- o DMAREN, MCRWR, DCNTCS
- o DMAEN, DKRQ, DKBG, DMA DATA

Floppy Disk Recalibration Procedure

This procedure uses the debugger program to manually check the operation of the floppy disk system when the floppy disk drive cannot boot diagnostics.

The procedure verifies the ability of the disk controller to execute the Restore and Seek commands. Data for these commands is shown in two forms: seek with and without verify. When the verify form is used with a formatted floppy disk, the WD2797 disk controller reads the track number from the disk and compares it with the number in its track register, thus verifying the ability of the controller to read data from the floppy disk. The no verify form can be used with an unformatted floppy disk.

1 Adjust the VCO capacitor.

- o Check the 1-MHz clock on the disk controller chip (pin 24)
- o Reset the floppy disk controller (pin 5) by setting MR (master reset) low and then setting it back high.

To do this, use the debugger program to write the following data to the disk control register:

Address	Data	MR Status (22M. Pin 19. WD2797)
4E0000	0000	Low (resets disk controller)
4E0000	0080	High (clears reset)

- o Ground the test pin.

Put a jumper across the two pins marked E4 and E5 next to the disk controller at 22M. This grounds pin 22, the test pin on the WD2797.

- o Adjust the frequency.

Put a oscilloscope on pin 16 and adjust the trimmer cap for a frequency of 250 kHz. After this is done, remove the jumper.

2 Verify that you can write to and read back from controller registers.

Logic Board Test Procedures

Using the following addresses, write data to each address and then read it back to check the disk controller's ability to store data in its internal registers. If this does not work, check the data and the read/write lines at the controller.

<u>Register</u>	<u>Address</u>
-----------------	----------------

Track	E10002
Data	E10006

- 3 Put a scratch floppy disk in the drive, select the drive, and turn on the motor by writing data FFE0 to address 4E0000.

The motor comes on and FDRIVE0, 17H (pin 6), will be high.

- 4 Issue the Restore command by writing FF0F (with verify) or FF03 (no verify) to address E10000.

If the head is not at track 0 already, it is driven there. After the command is executed, read the track register (E10002), which shows 0 (FF00).

Check that the controller (pin 39) generated an interrupt when the Restore command was completed.

- 5 Drive head to track 40 (inside track).
 - o Load hexadecimal 28 (decimal 40) into the data register by writing FF28 to address E10006.
 - o Issue the Seek command by writing FF13 (no verify) or FF1F (with verify) to address E10000.

During execution, a step pulse occurs at pin 15 each time the head moves one track.

When the Seek command is completed, the track register (E10002) contains 28 hex and a positive pulse appears on pin 39, indicating interrupt at command completion.

Table 4-4 lists the address, data, and WD2797 controller chip pins checked during this procedure:

Table 4-4 WD2797 Pin Listing

Address	Data	Pin	Notes
E10000	FF03	--	Restore command, no verify
E10000	FF0F	--	Restore command, with verify
E10000	FF13	--	Seek command, no verify
E10000	FF1F	--	Seek command, with verify
E10002	XXXX	--	Track register
E10006	XXXX	--	Data register
4E0000	FFE0	--	Data to select drive and motor
4E0000	FF00	--	Data to deselect drive, motor off
		39	Interrupt at end of command
		15	Step pulses during execution of Seek command

- 3 Put a scratch floppy disk in the drive, select the drive, and turn on the motor by writing data FFE0 to address 4E0000.

The motor will come on and FDRIVE0, 17H (pin 6), will be high.

- 4 Issue the Restore command by writing FF0F (with verify) or FF03 (no verify) to address E10000.

If the head is not at track 0 already, it is driven there. After the command is executed, read the track register (E10002), which shows 0 (FF00).

Check that the controller (pin 39) generated an interrupt when the Restore command was completed.

- 5 Drive head to track 40 (inside track).
 - o Load hexadecimal 28 (decimal 40) into the data register by writing FF28 to address E10006
 - o Issue the Seek command by writing FF13 (no verify) or FF1F (with verify) to address E10000.

During execution, a step pulse occurs at pin 15 each time the head moves one track.

Logic Board Test Procedures

When the Seek command is completed, the track register (E10002) contains 28 hex and a positive pulse appears on pin 39, indicating interrupt at command completion.

Floppy Disk Read Track Procedure

This procedure uses the debugger program to read information from a floppy disk for analyzing problems involving booting from the floppy disk drive.

- 1 Initialize the system by loading the following data at the addresses shown:

4A0000:	0	Sets DMA R/W* bit low (see sheet 16 of schematics)
4E0000:	0	Resets floppy disk controller
4E0000:	E0	Selects floppy disk drive and turns on motor

This step selects the disk drive and sets up the disk PAL for a floppy disk write to memory from disk. This has to be done only once unless you turn off the power or push the Reset button.

- 2 Load DMA address and word counters by writing the following data to the addresses shown:

4D0000:	0	
4D4000:	0	Sets starting address at 0
460000:	0	Shows C000 when 0 is written to this address
460000:	8000	

This enables a DMA write to memory. The transfer to memory starts from address 000000 in RAM.

Note

460000 shows C001 after you write 8000 to this address. This indicates that the DMAEN+ bit is set and the first byte has been moved. If you read address 0 at this point, it is different. These counters should be set up before any command that reads or writes information from a track or sector.

- 3 Issue the Read Track command to read either side 0 by writing E0 or side 1 by writing E2 to address E10000.

This causes track 0, side 0 or side 1, to be moved into the first 8KB of memory. The highest address that contains data from the track is about 187A (hex). The disk controller starts reading from the first index pulse after the command is issued and continues until the next index pulse.

IBM System 34 Format

<u>Number of Bytes</u>	<u>Hex Value of Byte Written</u>
80	4E
12	00
3	F6 (writes C2)
1	FC (index mark)
50	4E
-----*	
12	00
3	F5 (writes A1)
1	FE (ID address mark)
1	Track number (0-4C)
1	Side number (0 or 1)
1	Sector number (1-1A)
1	01 (sector length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (writes A1)
1	FB (data address mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
-----*	
598	4E

* Bracketed field is written 26 times.

- 4 Examine memory (see preceding table) starting at address 0 and look for the pattern of 80 4Es and 12 00s that precedes the index address mark of FC.

Logic Board Test Procedures

Note

The 4E pattern may look like 27, 96, or 39 at first, because the disk controller has not yet synchronized its data separator, which tells it which bit a byte starts with.

- 6 Next find the ID fields for the first sector. Look for an A1A1EB pattern.

The next byte after EB is the first byte of the six bytes in the ID field. The contents of the fields are:

- Byte 1: Track address 0-40 (decimal)
- Byte 2: Side number 0 or 1
- Byte 3: Sector address 1-26 (decimal)
- Byte 4: Sector length code
- Byte 5: CRC
- Byte 6: CRC

Seek Command

If you want to modify the preceding procedure to read a different track, simply load the data register with the track you want and issue the Seek command before issuing the Read Track command. Note that there are two forms of the Seek command: with and without verify. With verify, the command reads the track information from the disk and compares it with its internal track register. The maximum track number is 28 hex.

Read Address Command

If you want only to read the ID field, you can substitute the Read Address command for the Read Track command. With this command, you can read the first ID field after the index pulse. Because this command writes only six bytes, you can repeat the command without reloading the DMA counters. The data is six bytes higher in memory because the address counter advances with each execution.

Summary of addresses and data used in the foregoing procedure:

4A0000:	0	Sets DMA R/W*
4E0000:	0	Resets controller
4E0000:	E0	Selects controller and turns on motor
4D0000:	0	DMA address counter
4D4000:	0	DMA address counter
460000:	8000	DMA word counter, DMAEN+, IDMAR/W*
E10002:		Track register
E10004:		Sector register
E10006:		Data register

Summary of commands used to write to the floppy disk controller command register at address E10000:

1B:	Seek, no verify
1F:	Seek, with verify
E4:	Read Track side 0
E6:	Read Track side 1
C4:	Read Address side 0
C6:	Read Address side 1
8C:	Read Sector side 0
8E:	Read Sector side 1
AC:	Write Sector side 0
AE:	Write Sector side 1

Guidelines for using commands:

All commands:	Set DMA R/W*, reset controller, and select drive and head before executing first command and after any reset.
Seek:	Load data register with desired track number first.
Read Track:	Set up DMA counters first.
Read Address:	Set up DMA counters first.
Read/Write	Sector: Set up DMA counters and load sector number into sector register first.

Sector numbers start at 1. Tracks are 0-40 decimal or 28 hex.

Logic Board Test Procedures

Floppy Write Sector Procedure

This procedure writes data from the lowest 1/2 KB of memory to sector 1, track 0, side 0 of the floppy disk. Enter the following data at the addresses shown:

4A0000:	4000	Sets DMAR/W- high to read memory and write to disk
400000:	0	Resets floppy disk controller
4E0000:	E0	Selects floppy drive 0 and turns on motor
4D0000:	0	A1-A8 correspond to least significant 8 bits of DMA address
4D4000:	0	Sets starting address to 0; A1-A13 correspond to most significant 13 bits of DMA address
460000:	0	Shows C000
460000:	C000	Sets DMAEN D15 and IDMAR/W high; initializes DMA word count to 0 E10000: AC. Writes sector side 0

Initialize Floppy Program

This machine language program initializes the DMA bus interface and floppy disk controller to read sector 1, track 0, side 0 from a formatted floppy disk. To use the program, perform the following steps:

- 1 Load the program as shown below. Verify that it is entered correctly using the debugger DI command.

Note

The program is stored in video memory so that it is not overwritten by disk DMA.

420008:	33FC	
42000A:	0000	Resets disk drive
42000C:	004E	
42000E:	0000	
420010:	33FC	
420012:	00E0	Selects disk drive
420014:	004E	
420016:	0000	
420018:	33FC	
42001A:	0000	Sets DMA address least significant bits to 0
42001C:	004D	Uses address bits A1-A8
42001E:	0000	
420020:	33FC	
20022:	0000	Sets starting address most significant bits to 0
420024:	004D	Uses address bits A1-A13
420026:	4000	
420038:	4EF9	
42003A:	0080	Returns to debugger
42003C:	0EE0	

Note

This program starts storing data from sector 1 at RAM address 000000. You can change the starting address by changing the address data shown at 42026. For example, to change the starting address to 70000, change data for address 420026 to 4700. The third digit of this address 420026 to 4700. The third digit of this word is the fifth digit of the DMA address.

2 Execute the program by typing go 420000.

The debugger message scrolls on the screen.

3 Read sector 1 by writing 8C (the Read Sector command) to E10000.

4 Examine memory to see if the command has been executed.

Logic Board Test Procedures

Note

If you issue the Read Sector command a second time, the sector is read again but it is stored in the next 1/2 KB word of memory. You can fill as much memory as you like by repeating the Read Sector command. Each time the Read Sector command is repeated, the DMA word counter at 460000 increments by 1/4 KB.

DMA Looping Program

The following machine language program uses a loop instruction to test the DMA bus interface. It produces a continuous disk bus request, grant, and acknowledge waveform. The program fills the 2 MB of memory that can be accessed by DMA with the same data.

420100:	33FC	
420102:	0000	
420104:	004A	Sets DMA R/W bit low to write to memory
420106:	0000	
420108:	33FC	
42010A:	0000	Sets DMA enable low
42010C:	0046	
42010E:	0000	
420110:	33FC	
420112:	8000	Toggles DMA enable high
420114:	0046	
420116:	0000	
420038:	60EE	Branch always

Hard Disk Registers

This section provides general information that is to be used in the procedures involving the hard disk drive. Addresses 4A0000 and 4E0000 are the addresses of the disk control and miscellaneous control registers. These registers must be set up before any command is written to the disk controller.

Summary of addresses and data written to the disk control and miscellaneous registers:

4A0000:	0000	Sets bit 14 low for DMA read disk and write to memory
4A0000:	8000	Sets bit 14 high for DMA read memory and write to disk (see sheet 15 of schematics for circuits)
4E0000:	FF00	Resets hard disk controller (see sheet 11)
4E0000:	FF19	Selects drive 0, head 0 (see sheet 11) and clears reset

To set the DMA address counter to start a DMA transfer at memory address 0, write 0 to addresses 4D0000 and 4D4000. Do this before each Read or Write Sector command.

To set the DMA word counter and enable DMA write, write the following data to the address shown:

460000:	0	Sets enable low
460000:	8000	Sets DMAEN high and selects DMA write

To initialize the WD1010 internal registers, write the following data to the addresses shown:

E00004:	01	Sector count (number of sectors to be transferred)
E00006:	0000	Sector number (sector to be transferred)
E00008:	FF64	Cylinder, least significant 8 bits
E0000A:	FF02	Cylinder high (only bits 0 and 1 are used)
E0000C:	20	Size drive head (SDH), head 0, drive 1, 512 bytes/sector

WD1010 Command Register (E0000E)

Table 4-5 lists the WD1010 command register bit definitions:

Logic Board Test Procedures

Table 4-5 Bit Number

Command	7	6	5	4	3	2	1	0_
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read								
Sector	0	0	1	0	I	M	0	T
Write								
Sector	0	0	1	1	0	M	0	T
Scan ID	0	1	0	0	0	0	0	T
Write								
Format	0	1	0	1	0	0	0	0

R3-R0 = Step rate for head movement

F = 7.5 ms

0 = 35 us

I = Interrupt enable

I = 0 Interrupts at BDRQ time

I = 1 Interrupts at end of command

M = Multiple sector flag

M = 0 Transfers one sector

M = 1 Transfers multiple sectors

T = 0 Enables retries

T = 1 Disables retries

Commands in Hexadecimal

The left or most significant digit selects the command. The right or least significant digit selects the options described in the command register table above and in the following tables.

Restore = 1X, where X is a value from 0 through F depending on
step rate

Seek = 7X

Read Sector = 2X

Table 4-6 Read Sector Commands

Read Sector	I	M	T
20	0	0	0
21	0	0	1
24	0	1	0
25	0	1	1
28	1	0	0
29	1	0	0
2C	1	1	0
2D	1	1	1

Requirements to successfully complete the Read Sector command:

- o Ready input must be asserted from the disk drive.
- o Seek complete must be asserted at the end of a Seek command. A rising edge on this input informs the WD1010 when head settling time has expired.
- o Cylinder and head numbers must match.
- o No CRC error or bad block must be detected.
- o Data address mark must be found.

Logic Board Test Procedures

Write Sector = 3X

Table 4-7 Write Sector Commands

Write Sector	I	M	T
30	0	0	0
31	0	0	0
34	0	1	0
35	0	1	1
38	1	0	0
39	1	0	0
3C	1	1	0
3D	1	1	1

Scan ID = 80 or 81, where 80 is the interrupt at DBRQ and 81 is the interrupt at the end of the command.

Table 4-8 SDH Byte Register (E0000C, Read/Write)

SDH Byte Register			
Bit Number			Head Selected
2	1	0	
0	0	0	Head 0
0	0	1	Head 1
0	1	0	Head 2
0	1	1	Head 3
1	0	0	Head 4
1	0	1	Head 5
1	1	0	Head 6
1	1	1	Head 7
Bit Number			Drive Selected
4	3		
0	0		Drive 1
0	1		Drive 2
1	0		Drive 3
1	1		Drive 4
Bit Number			Size Selected
6	5		
0	0		256 bytes/sector
0	1		512 bytes/sector
1	0		1024 bytes/sector
1	1		128 bytes/sector

Bit 7, the extension bit, extends the data field by seven bytes when ECC codes are used. CRC is not appended to the end of the data field. The SDH byte is written into the ID field during format.

Write Precompensation Register (E00002, Write Only)

The value 00-FF loaded into this register is internally multiplied by 4 to specify the cylinder where RWC is asserted. A value of FF always causes RWC to be low, no matter what cylinder number is used.

Logic Board Test Procedures

Error Register (E00002, Read Only)

- Bit 7: Bad block detect, used for bad sector mapping.
- Bit 6: CRC error.
- Bit 5: Forced to 0.
- Bit 4: ID not found. This bit is set to indicate that the correct cylinder, head, sector number, or size parameter could not be found or that CRC error occurred on the ID field. This bit is set on the first failure and remains set even if the error is recovered on a retry. When recovery is unsuccessful, the error status bit is set also.
- Bit 3: Forced to 0.
- Bit 2: Aborted command. This bit is set if the command is issued while the DRDY is deasserted or the WF is asserted. The aborted command bit is also set if an undefined command code is written into the command register.
- Bit 1: Track 0 error. This bit is set only by the Restore command. It indicates that TK000 has not gone active after the issuance of 1KB of stepping pulses.
- Bit 0: Data address mark not found. This bit is set during a Read Sector command if the data address mark is not found after the proper sector ID is read.

Status Register (E0000E, Read Only)

- Bit 7: Busy. This bit is set whenever the WD1010 is accessing the disk. Commands should not be loaded into the command register while the busy is set.
- Bit 6: Ready.
- Bit 5: Write fault.
- Bit 4: Seek complete.
- Bit 3: Data request.
- Bit 2: Reserved, forced to 0.
- Bit 1: Command in progress.
- Bit 0: Error. This bit indicates that a nonrecoverable error has occurred. If the host reads the status and finds this bit set, it must read the error register (E00002) to determine the type of error written into the error register.

Hard Disk Recalibration Procedure

The following procedure uses the debugger program to verify the ability of the hard disk controller to execute the Restore and Seek commands and the ability of the data separator to produce a proper clock and data stream.

- 1 Write the following data in the sequence listed using the debugger program:

Disk control register, reset: 4E0000: FF00
Disk control register, select drive: 4E0000: FF19

- 2 After writing this data, verify the following signal conditions:

- o At chip 17K (pin 9), a logic low indicates that drive 0 has been selected
- o At chip 17K (pin 3), a logic low indicates that hard disk drive head 0 has been selected
- o At chip 18K (pin 5), index pulses are present
- o At chip 18K (pin 11), a logic low indicates that the drive is ready
- o At chip 16M (pin 9), separated data from the data separator is present
- o At chip 13K (pin 3), data from the hard disk drive is present.

- 3 Issue the Restore command by writing FF1F to address E0000E.

This command causes the stepping motor on the drive to bring the head back to cylinder 0 if it is not already there.

After this data is written to the WD1010 command register, the data you read back on the screen is FF50. This is the contents of the disk controller's status register, and it indicates that D6, the ready bit, and D4, the seek complete bit, are both high. When D6 is high, it indicates that the disk controller is receiving a logic high on its RDY pin 28. When D4 is high, it indicates that a seek initiated by the last command has been completed successfully.

- 4 Write the following reset and drive select data to the disk control register to reset the controller:

Disk control register, reset: 4E0000: FF00
Disk control register, select drive: 4E0000: FF19

Logic Board Test Procedures

- 5 Load the cylinder register as shown below (these are read/write registers, so you should read back the same data you write):

Cylinder number low (614): E00008: FF64

This register holds the eight least significant bits of the cylinder number.

Cylinder number high (614): E0000A: FF02

Bits 0 and 1 are the two most significant bits of the cylinder number.

- 6 Issue the Seek command, which causes the stepping motor to rotate until the head is at cylinder 614.

Seek command: E0000E: FF7F

Procedures for Reading/Writing Data to Any Sector

Using the debugger program, the next two procedures make it possible to write any desired data to any selected sector on the hard disk and read it back to verify that it was written properly. These procedures use the Read Sector, Write Sector, Seek, and Scan ID commands of the WD1010 controller. The error register bits generated by the WD1010 are listed as well as the signals to check when a board failure prevents these procedures from executing properly.

Read Data to Any Sector

- 1 Set the DMA address counter:

4D0000: 0

4D4000: 0

- 2 Set DMA write, select the drive, and restore the head to track 0:

4A0000: 0 Sets bit 14 low, DMA write to memory from disk

4E0000: 0 Resets the disk controller

4E0000: 19 Selects drive 0, head 1

E0000E: 1F Restore command, returns the head to track 0

- 3 Set the DMA word counter and toggle DMA enable:

460000: 0 Reads C000
460000: 8000 Reads C001

- 4 Clear memory by putting 0's in the first 16 words of memory at addresses 0h-2h and 1F0-1FF.

- 5 Load the hard disk controller registers by writing the following data to the addresses shown:

E00002: 0 Write compensation register
E00004: 1 Sector count register (selects the number of sectors to read)
E00006: 0 Sector number register (selects the sector to read)
E00008: FF Least significant byte of cylinder number (cylinder 255 selected as an example)
E0000A: 0 D0 and D1 are most significant bits of cylinder number

- 6 Issue the Seek command by writing 7F to address E0000E.

You read back D2 and the stepping motor rotates. D2 indicates that the command has executed with no errors.

- 7 Issue the Scan ID command to update the SHD register by writing 41 to address E0000E.

You read back D2, indicating successful completion.

- 8 Check the SDH register by reading address E0000C.

It contains FF21, which indicates that 512 bytes per sector and head 1 have been selected.

- 9 Write 28 (Read Sector command) to address E0000E.

It reads back D2. Check the contents of memory to see that the data has been moved from disk. If you do not read D2 after issuing this command, read E00002, the error register, and determine the error. If you write 28 to E0000E again, the command is executed again, but the data is transferred to the next 1/2 KB of memory from address 000200 to 000300. Each time the command is repeated, the DMA count register at 460000 shows another 1/2 KB of data moved. After the first execution, it shows C101; after the second execution, it shows C201, and so on.

Logic Board Test Procedures

Write Data to Any Sector

This procedure can be used to write data to any selected sector of the hard disk drive from the first 1/2 KB of memory. To execute the procedure, use the debugger program to write the data to the addresses shown.

- 1 Set the DMA write bit, select the drive, and restore the head to track 0:

4A0000:	4000	Sets bit 14 high, DMA write to disk from memory
4E0000:	0	Resets disk controller
4E0000:	19	Selects drive 0, head 1
E0000E:	1F	Restore command

- 2 Set the DMA address counter to 0:

4D0000:	0
4D4000:	0

- 3 Set the DMA word counter and toggle DMA enable:

460000:	0	Reads C000
460000:	C000	Reads C001, bit 15 is DMAEN, bit 14 is R/W*

- 4 Load an arbitrary data pattern in the first 16 words of memory at addresses 0h-2h.

- 5 Load the hard disk controller registers:

E00002:	0	Write compensation register
E00004:	1	Sector count register (selects the number of sectors to read)
E00006:	0	Sector number register (selects the sector to read)
E00008:	FF	Least significant byte of cylinder number (cylinder 255 selected as an example)
E0000A:	0	D0 and D1 are most significant bits of cylinder number

- 6 Issue the Seek command:

E0000E:	7F
---------	----

It reads back D2 and the stepping motor rotates. D2 indicates that the command has executed with no errors.

- 7 Issue the Scan ID command to update the SDH register:

E0000E: 41

It reads back D2, indicating successful completion.

- 8 Check the SDH register by reading E0000C.

It contains FF21, which indicates that 512 bytes per sector and head 1 have been selected.

- 9 Issue the Write Sector command by writing 35 to address E0000E, and then use the read sector procedure above to verify that the data has been moved to disk.

After the Write Sector command has been issued, address E0000E shows DA if the command executes without error. If it does not execute properly, read address E00002, the error register, to determine the error.

Write fault and DRDY lines are checked by the controller during command execution.

Signals to Check if Procedures do not Execute

DRDY (IC21H, pin 28) must be asserted after the drive is selected in step 1.

SC (IC21H, pin 32) must be asserted from the drive when a Seek command is completed.

Unseparated data from the drive must appear at IC13K (pin 3) and separated data must appear at IC16M (pin 9) during a Read Sector command.

WFAULT (IC21H, pin 30) must not be asserted from the disk drive.

INTRQ (IC21H, pin 3) must be asserted at the end of a command and must be latched into the line printer status register at IC15P (pin 15).

TK000 (IC21H, pin 31) must be asserted after the Restore command is executed.

INDEX pulses (IC21H, pin 29) from the drive must appear after the drive is selected.

Logic Board Test Procedures

Disk RE (IC21H, pin 6) and WE (IC21H, pin 7) must be asserted during command execution.

TFER (IC24H, pin 18) must occur for each byte transferred. For every other TFER, there must be a DKBG (IC25B, pin 17) and a DKBGA (IC26F, pin 8).

Bit D0 of the WD1010 status register at address E0000E must be low after any command is issued. If it is not, read E00002, the error register, to determine the error.

Hard Disk Data Separator Test

This test verifies proper operation of the hard disk data separator and its component circuits. The test requires a running system with debugger PROMs installed, a serial terminal connected to the serial port, an oscilloscope, and a frequency counter. The hard disk data separator is shown on sheet 12 of the schematics.

The circuits that make up the data separator are:

- o Voltage-controlled oscillator (output at IC14N, pin 10)
- o Phase detector (outputs at IC18M, pins 11 and 8)
- o Loop filter (output at IC17N, pin 1)
- o Data run one shot (output at IC13N, pin 13)
- o Data separation PAL (outputs at IC14M, pins 19 and 12)

To perform this test:

- 1 Select the hard disk drive.

Before the data separator can be tested, the hard disk drive must be selected to provide 5-MHz data and clock input to data separation PAL IC14M (pin 3). To select the drive and cause the drive to send data, push the Reset button and then use the debugger program to write 19 hex to address 4E0000. This causes pins 9 and 3 of IC17K (shown on sheet 11) to go low. These signals are sent to the hard disk drive, which responds by turning on its LED and generating the following signals (shown on sheet 11):

- o DRDY from the drive goes low at IC18K (pin 11)
- o INDEX pulses appear at IC18K (pin 5)
- o TK000 goes low at IC18K (pin 3)
- o SC goes low at IC18K (pin 13)

2 Check the data separator input and output.

Use a oscilloscope to check the input to the data separation PAL on sheet 12 at IC14M (pin 3). It contains 5-MHz data and clock pulses coming from the hard disk drive. Then check the output of the data separator at IC16M (pin 9), which shows 5 MHz. The DRUN signal at IC13N (pin 15) is high. RCLK at IC14M (pin 12) shows 5 MHz.

If these results are not obtained, test the individual circuits that make up the data separator using the following procedures (steps 3-5):

3 Check the voltage-controlled oscillator.

The voltage-controlled oscillator is IC14N. First check pin 11, the enable input; it is low to enable the oscillator. Next ground pin 1, the voltage control input, forcing the output frequency to a minimum of 3-4 MHz. Then connect pin 1 to 5 volts, forcing the output frequency to a maximum of 17-18 MHz.

4 Check the pullup and pulldown circuits and the loop filter.

To test pullup, ground pin 11 of IC18M, the pullup circuit. This saturates Q7. Its collector goes to +5 volts, causing the inverting input of IC17N (pin 6) to be +5 volts and the noninverting input to be +3.75 volts. This +3.75 volts results from the voltage drop across R67 to the voltage divider made up of R96 and R97. Thus the output at pin 7 drops to -12 volts. The section of 17N with output at pin 1 is connected as an inverting amplifier with a gain equal to the ratio of R65 to RP24, or about -2, and its input is fed from IC17N (pin 7). With an input of -12 volts, the output is driven to the positive supply voltage of +5 volts. This drives the output of the VCO IC14N (pin 10) to a maximum of about 17 MHz. Enable pin 11 must be low for the VCO to work.

To test pulldown, ground the output of the pulldown circuit at IC18M (pin 8). This causes the inverting input at IC17N (pin 6) to drop to 0 and the noninverting input to be +1.25. Thus the output at pin 7 is +5 volts, causing the output of the inverting amplifier to be -12 volts. This output results in -0.66 volts at IC14N (pin 1) of the VCO. The -0.66 volts is the output of voltage divider R64 and RP24. This voltage divider applies $1/3$ of the -12 volts from the inverting amplifier output at IC17N (pin 1) plus $2/3$ of the +5 volts connected to RP24. The total is -0.66 volts. The result is that the VCO outputs a minimum frequency of 3-4 MHz.

Logic Board Test Procedures

During normal operation, the capacitor C253 provides an integrating action. To check this, connect a oscilloscope on the output at IC17N (pin 7) when the VCO is locked on a 10-MHz output. The input to the VCO is about +2 volts. To obtain this, the output of the integrator at IC17N (pin 7) is about -4 volts. Each time a pullup pulse is generated, the voltage across C253 starts to swing negative at a rate calculated by dividing the current through R68 by the value of C253, or about $2.5 \text{ mA} / 0.01 \text{ uFd} = 250,000 \text{ volts per second}$. Since typical pullup or pulldown pulses last only 10-20 ns, the output can change by about 5 mV for each pullup or pulldown pulse.

5 Check the phase detector.

The phase detector has a 5-MHz input from IC14M (pin 1) of the data separator PAL and a 5-MHz input from IC14M (pin 19). The 50-ns delay circuit together with the data flipflop output IC15K (pin 9) generates a 25-ns pulse at IC17M (pin 11). Pulses of 10 MHz are applied to IC16M (pin 11).

Dialer Test

The following addresses and data turn on the tone generator in the dialer chip and send tones to the speaker in the monitor. To turn the tone off, write the second address twice.

4B0560:	0	
4B0800:	0	Turns on maximum volume ringing
4B0500:	0	
4B0802:	0	Dual tone to speaker
4B0540:	0	
4B0802:	0	Single tone to speaker
4B0548:	0	
4B0802:	0	Single tone to speaker

Waveform Timing Analysis Procedure

This procedure checks signal generation and signal timing during various bus cycles of the logic board.

Special tools required include:

- o HP1630D logic analyzer
- o Piggyback extender cables
- o Floppy diagnostics disk

Logic Analyzer Setup

- 1 Disassemble the UNIX PC to gain access to the logic board.
- 2 Install external cables to the piggyback board (if present).
- 3 Set up the HP1630D logic analyzer as follows:
 - o Apply power by depressing the line switch in the upper-right corner. The logic analyzer comes up in the system mode.
 - o In system mode, select timing mode by moving the down-arrow cursor key to the second line (- 16).
 - o Depress the format key and create the following labels:

LABEL	POL	POD1	POD0
1PCK	+		*
LDS	+		*
UDS	+		*
DTACK	+		*
AS	+		*
R/W	+		*
ADDEN	+		*
DBEN	+		*
RAMEN	+	*	

- o Go to trace mode and set the trace on the AS signal by putting a 0 under AS.

Logic Board Test Procedures

- o Connect the signal probes from POD1 and POD0 to the following locations on the logic board:

Signal	Chip	Pin	Schematic
1PCK	14E	15	Sheet 5
LDS	14E	8	Sheet 5
UDS	14E	7	Sheet 5
DTACK	14E	10	Sheet 5
AS	14E	6	Sheet 5
R/W	14E	9	Sheet 5
ADDEN	17F	19	Sheet 5
DBEN	13D	9	Sheet 5
RAMEN	12C	19	Sheet 20

- 4 When the connections are made and the trace is set, insert the floppy diagnostics disk and power up the system.
- 5 When the disk has booted, depress the Run button on the logic analyzer.

This causes a waveform to be stored.

Typical Waveforms

The following waveforms show examples of a fast-cycle read operation. The first example shows the timing of AS-, which is approximately 130 ns after the beginning of the machine cycle.

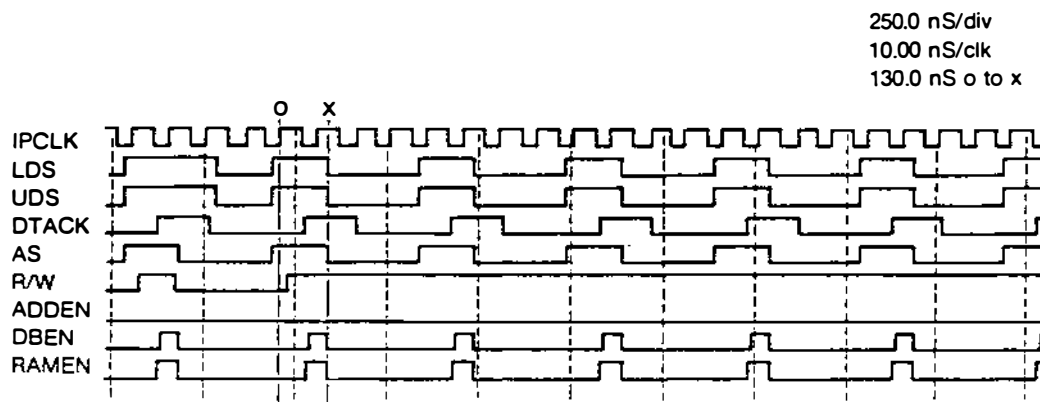


Figure 4-1 Timing of AS- (130 ns)

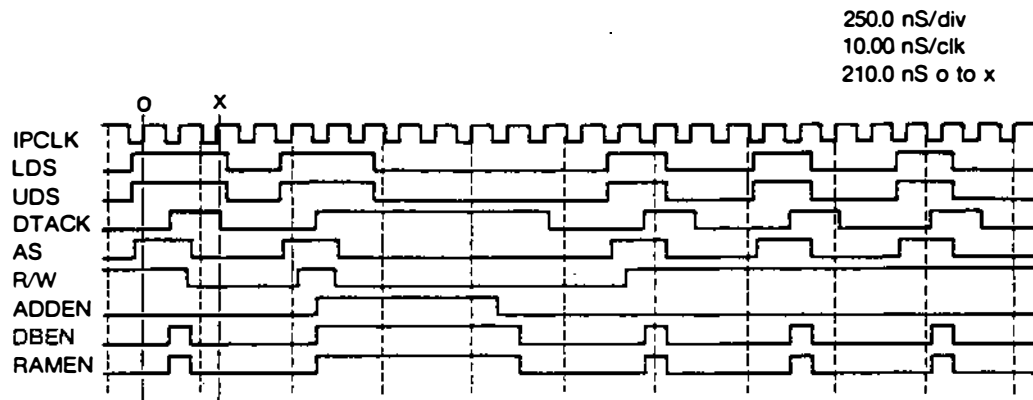


Figure 4-2 Timing of DTACK (210 ns)

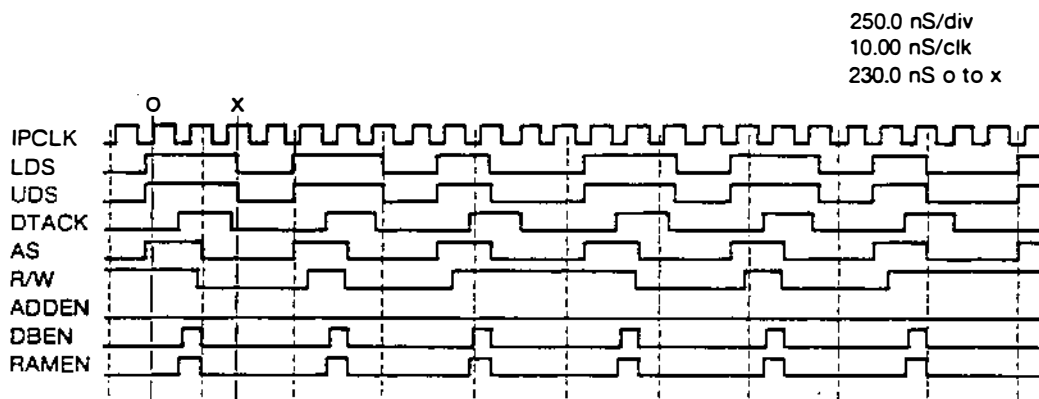


Figure 4-3 Timing of LDS and UDS (230 ns)

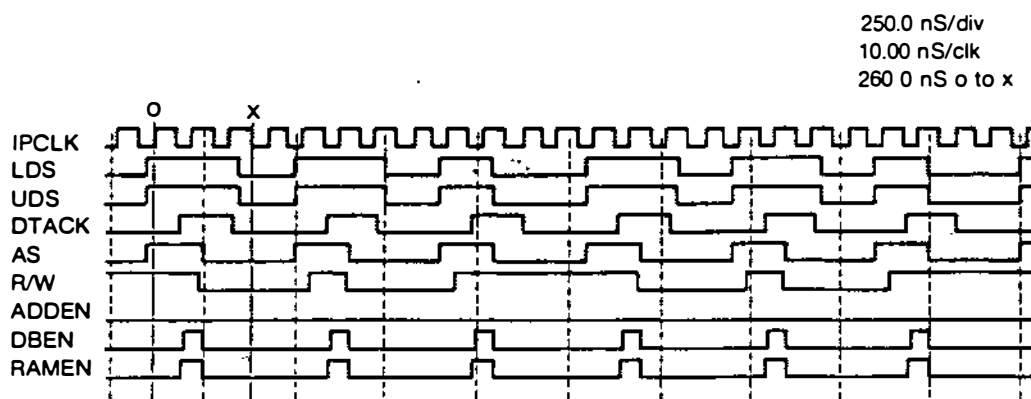


Figure 4-4 DTACK Latched by Processor (260 ns)

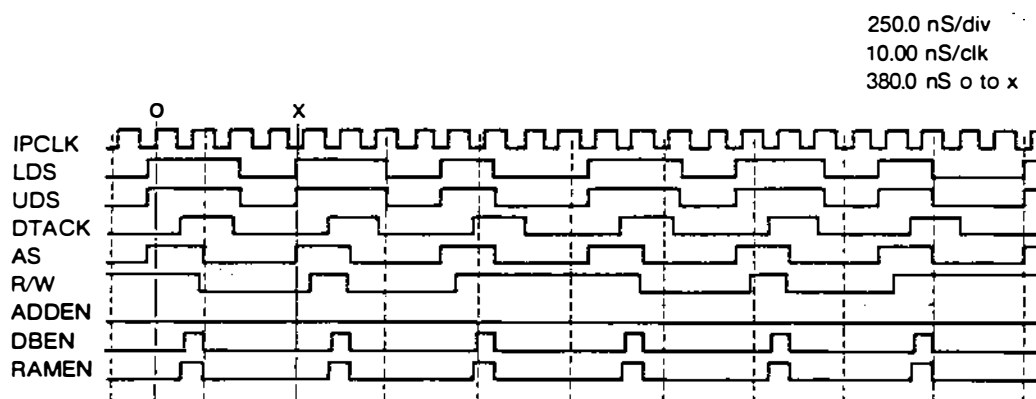


Figure 4-5 AS, LDS, and UDS Deasserted by Trailing Edge of Next IPCLK (380 ns)

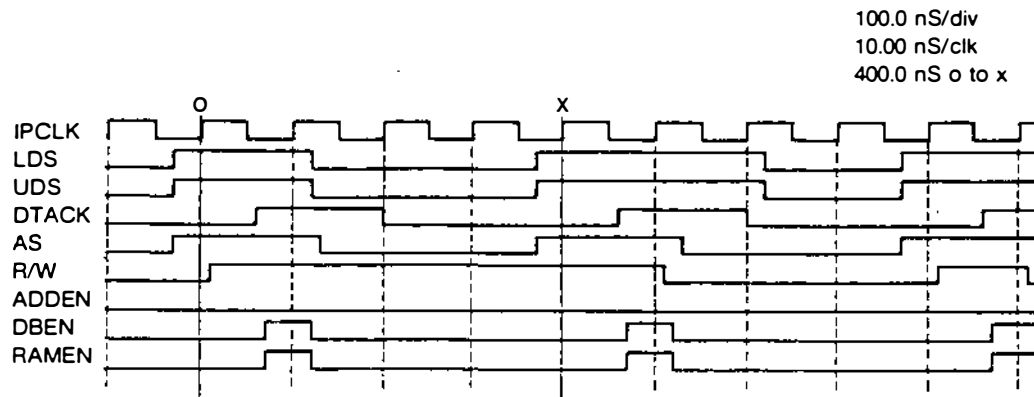


Figure 4-6 Length of Machine Cycle (400 ns)

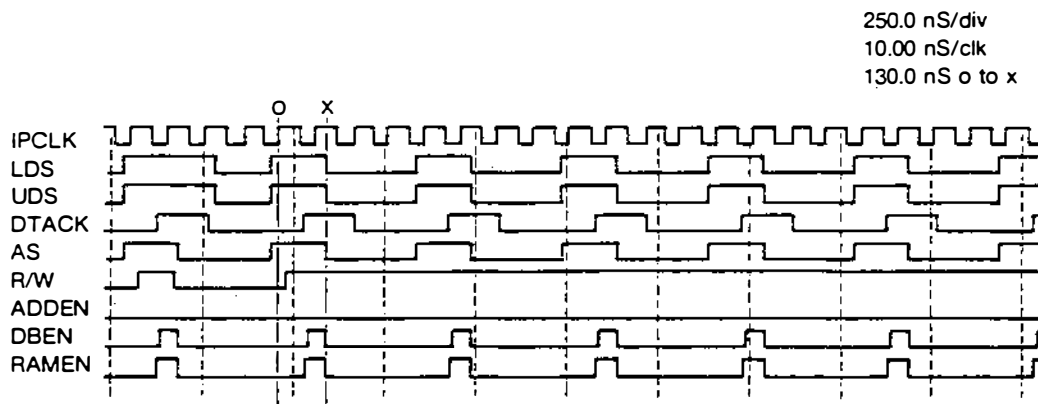


Figure 4-7 Timing of LDS and UDS During a Read Operation (130 ns)

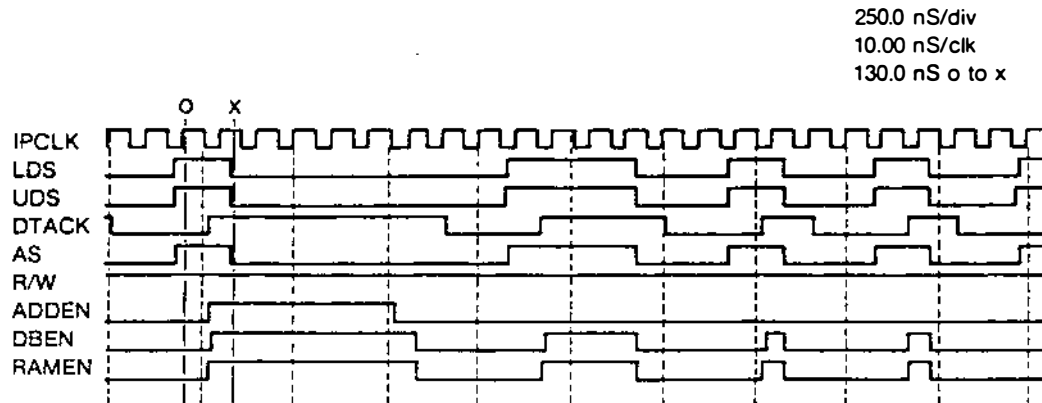


Figure 4-8 Slow Cycle Timing of AS (130 ns)

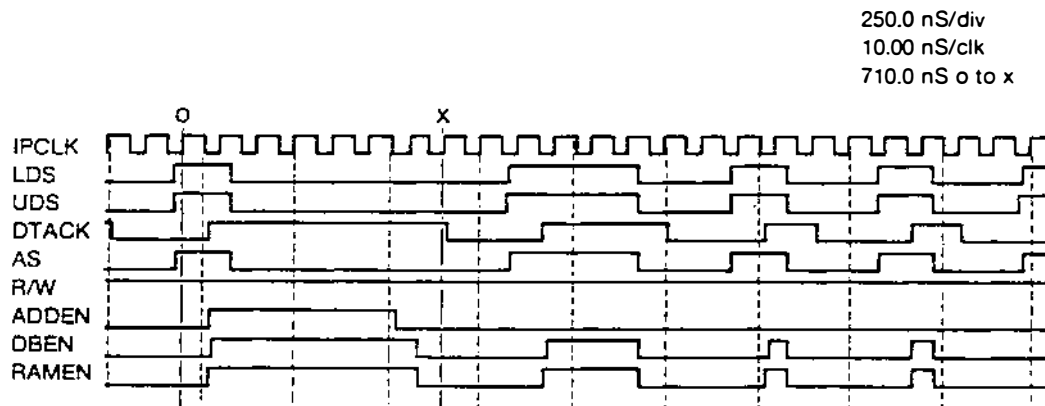


Figure 4-9 Timing of DTACK (710 ns)

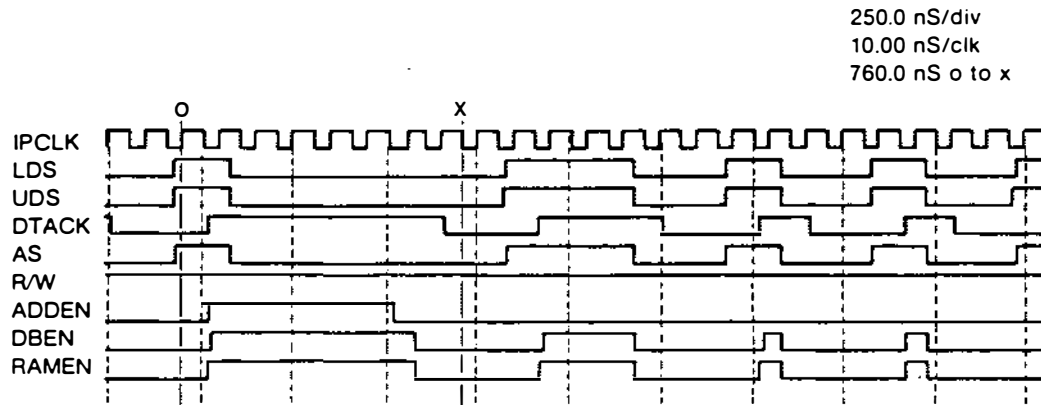


Figure 4-10 DTACK Latched by Processor (760 ns)

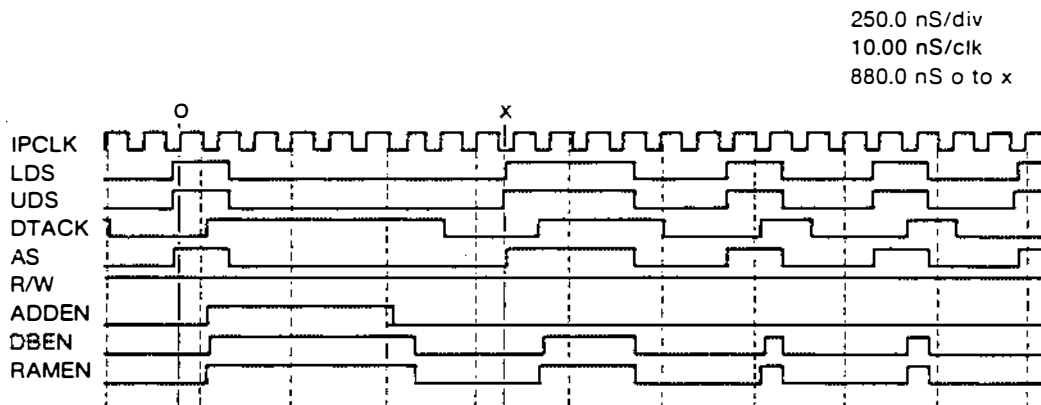


Figure 4-11 AS, LDS, and UDS Deasserted by Trailing Edge of Next IPCK (880 ns)

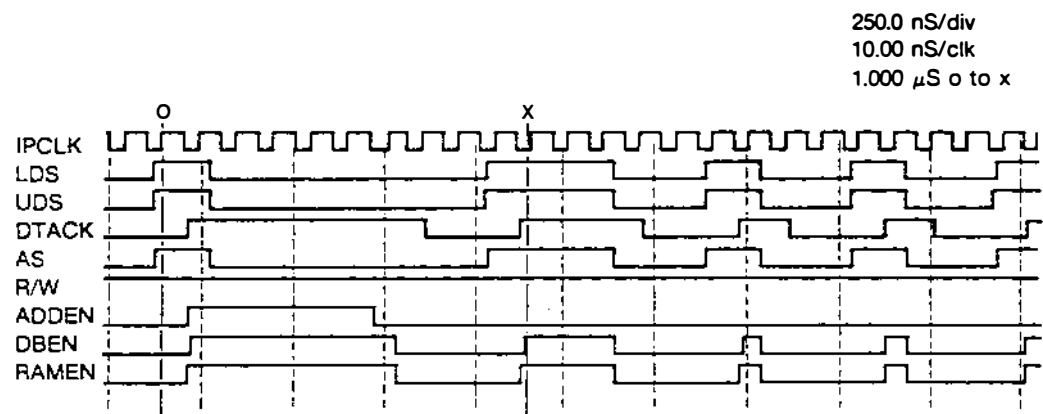


Figure 4-12 Slow Cycle Ends (Complete Cycle = 1.0 μ s)

68010 Timing Summary

The following waveforms show examples of a 68010 write cycle and a 68010 read cycle summary.

The 68010 to DRAM write cycle timing summary as shown in figure 4-13 is as follows:

- 1 DTACK goes low before the trailing edge of state 4. This is a high to low clock pulse. From this reference point, the rest of the timing state are identified. The complete cycle takes place in 4 clock cycles of 100 ns each. Address line A23 goes low.
- 2 Address is tristate during S0 and becomes valid during state 1. A23 is valid at the end of state 1.
- 3 During state 2 the address strobe goes low and r/w (read-write) goes low.
- 4 When A23 goes low it causes the following timing events to occur.

On sheet 3 of the schematic, 19K pin 6 goes low at next 2 PCK+ going hi. This is the start of state 2.

21E pin 5 goes low generating ENRAS*. The propagation delay 19K and 21E causes ENRAS* going low to be delayed up to 12 ns after the rising edge of S1.

28 to 32 ns after ENRAS* goes low T30* goes low.

- 5 On sheet 17 of the schematic, when T30* goes low, 3 to 8 ns later the RAS input to the DRAM's goes low. RAS going low strobes the row address from A3 to A11 into the DRAM's. 57 to 63 ns after ENRAS* goes low T60* goes low.
- 6 On sheet 18 of the schematic, when T60* goes low, the select inputs to the 74F25B multiplexers switch the address input to DRAM's from row address to column address. 4 to 11 ns after T60* goes low the output of the multiplexers will be valid. Column address comes from the MAP rams.

The MAP rams receive valid address 2.5 to 6 ns after the start of state 2. The access time of the MAP rams is 35 ns.

The MA12-MA21 address output of the MAP ram is valid at the input to the multiplexers 37.5 to 41 ns after the start of state 2.

Logic Board Test Procedures

- 7 On sheet 3 of the schematic, 87.5 to 100.5 ns after ENRAS* goes low, 19F9 goes hi. This causes 27F8 to go hi after 27N5 goes low generating DTACK* to the 68010. The propagation delay of the gates generating DTACK and variations in delay adds about 13 to 31 ns to the 90 ns output of the delay line. Thus, DTACK goes low at the 68010 input pin 10 between 100 and 126.5 ns after the start of state 2.
- 8 On sheet 5 of the schematic, DTACK* arrives at the processor about 24.5 to 50 ns before the falling edge of S4. DTACK* must go low before the falling edge of S4 to prevent the 68010 from inserting wait states. Output data from the processor is valid before the end of S3.
- 9 On sheet 16 of the schematic, T120* goes low 114 to 126 ns after NRAS* goes low. A low T120* causes 25K pin 6 to go hi which in turn makes 26M pin 11 hi and further 25F18 hi causing ENCAS+ to be hi. The delay of these gates, makes ENCAS+ hi between 13 and 37 ns after T120* goes low. Thus, the CAS input to the DRAM's goes low between 136 and 176 ns after the start of state 2.

Data from the 68010 is stable at the latest by the rising edge of state 4. It takes a maximum of 14 ns to pass data through the 74F245 data buffers. Data from the processor arrives at least 29 ns before it is strobed into the DRAM's by CAS.

- 10 On sheet 3 of the schematic, T120 going low causes 19F pin 7 to go hi and 28F pin 6 goes hi, k18G pin 8 goes low and 16K pin 13 goes hi. The rising edge of state 6 clocks MMUWREN+ hi. Variation in propagation time causes 16K pin 13 to go hi 122 to 145 ns after the rising edge of state 1.

16K pin 13 is hi a minimum of 55 ns before the rising edge of S6. MMUWREN+ going hi sets 18H4 hi. The falling edge of S7 clocks 18H3 hi resetting MMUWREN+.
- 11 On sheet 2 of the schematic, during the time that MMUWREN+ is hi 25C pin 6 is low. This generates MMUWR*. MMUWR* enables tristate buffers 24F which output the new page status for the MAP RAM's.
- 12 On sheet 16 of the schematic, MMUWR* puts a low on the W* input to the 19C and 20C MAP RAM's. This causes the new page status to be written to the MAP RAM's during S6.

-
- 13 On sheet 3 of the schematic, MMUWREN+ hi causes 16K pin 13 to go low. The rising edge of S7 then clocks 18H pin 3 hi setting 21E pin 4 hi. If A23 is low on the next rising clock pulse the memory cycle can start over.
 - 14 On sheet 2 of the schematic, during a 68010 access to I/O address space PA22 is hi and CASEN+ is not hi.

68010 to DRAM write cycle summary:

A23 before the leading edge of S2
 ENRAS* low 6 to 13 ns after S2's leading edge
 T30* goes low 37 to 51 ns after S2's leading edge
 DRAM RAS 37-51 ns after S2's leading edge
 DRAM ROW ADDRESS 5 to 12 ns after S2's leading edge
 DRAM ROW ADDRESS worst case setup time 23 ns
 T60* 63 to 75 ns after S2's leading edge
 T90* 91.5 to 106.5 ns after S2's leading edge
 DTACK* 100 to 126.5 ns after S2's leading edge
 T120* 120 to 139 ns after S2's leading edge
 DRAM CAS 136 to 176 ns after S2's leading edge
 DRAM COLUMN ADDRESS to MUX input 37.5 to 41 ns after S2's leading edge
 COLUMN ADDRESS set up before select input to MUX 22
 COLUMN ADDRESS TO DRAM 67 to 86 ns after S2's leading edge
 COLUMN ADDRESS SET UP before CAS 55 ns (write cycle)
 DATA to DRAM 205 to 213 ns after S2's leading edge
 DRAM DATA SET UP 29 ns.

Logic Board Test Procedures

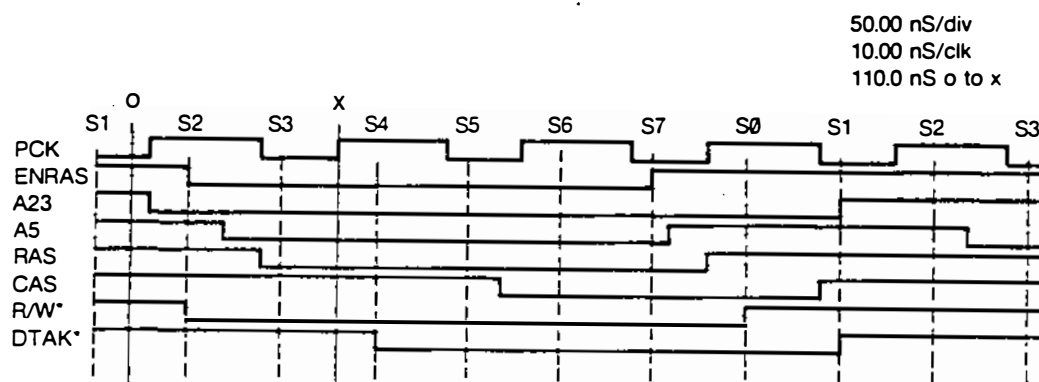


Figure 4-13 68010 to DRAM Write Cycle

The 68010 read cycle timing summary as shown in figure 4-14 is as follows:

- 1 During a read cycle CAS to the DRAM's is generated earlier than during a write cycle because data from the DRAM chips is not valid until 60 ns after CAS or 120 ns after RAS.
- 2 CAS must go low before DTAK to allow time for data from DRAM to be stable at the input of the 68010. During a read the opposite is true. CAS must not go low until data from the 68010 data bus is stable at the input to the DRAM's.

Read Cycle Summary:

CAS to DRAM 94.5 to 115.5 ns after S2 leading edge.
DRAM read column address set up 14.5 ns.
Data from DRAM valid 156.5 to 189.5 ns.
68010 data read set up time 60 ns.
Minimum row address hold 21 ns - 15 ns chip = 6ns.

Logic Board Test Procedures

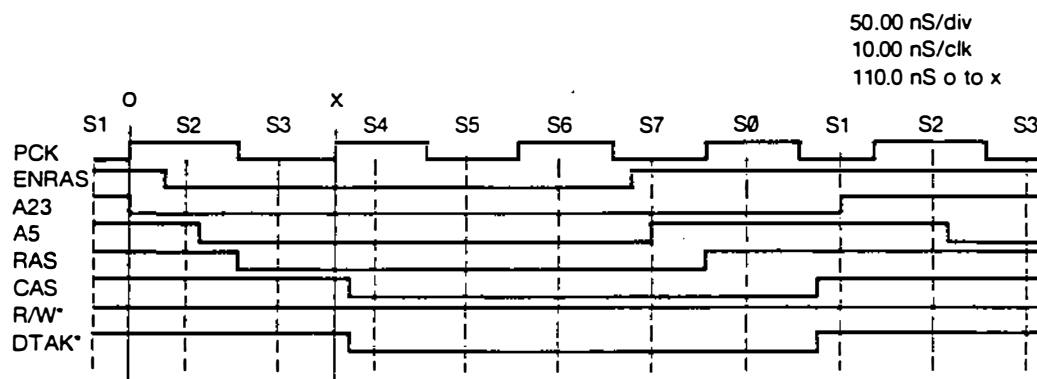


Figure 4-14 68010 Read Cycle Summary

A PAL Equations

The UNIX PC uses four programmable array logic (PAL) integrated circuits: the disk, arbitor, and memory management unit PALs are shown on sheet 2; the data separator PAL is shown on sheet 12.

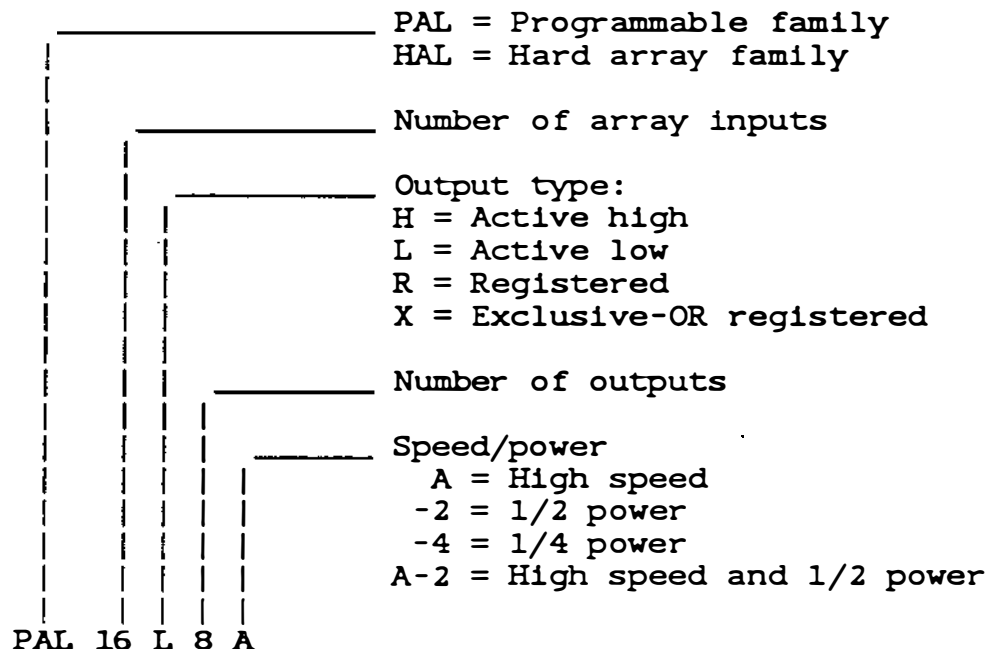
The operation of a PAL is described by a logic equation in a PAL listing. The listing is used to determine the correct logic levels of the outputs with a given set of inputs.

PROM's have been widely used by system designers to implement firmware. The PAL extends this programmable flexibility by utilizing fusible link technology to implement logic functions.

The PAL implements the familiar sum of products logic by using a programmable AND array whose outputs feed a fixed OR array. Since the sum of products form can express any Boolean transfer function, the PAL circuit uses are limited only by the number of terms available in the AND/OR arrays. PALs come in different sizes to allow for effective logic optimization.

PALs can be programmed in most standard PROM programmers with the addition of a PAL personality card.

The PAL identification number is broken down as follows:



PAL Equations

Arbitor: PAL 16R8A (Sheet 2: C-6)

Pin Signal Names

Pin Number	Mnemonic	Description
1	PCK*	Input: processor clock
2	RFRQ*	Input: refresh request
3	EXP3RQ*	Input: expansion board 3 request
4	DKRQ*	Input: disk bus request
5	EXP2RQ*	Input: expansion board 2 request
6	EXP1RQ*	Input: expansion board 1 request
7	EXP0RQ*	Input: expansion board 0 bus request
8	BGACK*	Input: bus grant acknowledge
9	ENRAS*	Input: enable row address strobe
10	(Ground)	-----
11	OE	Output enable
12	NRF/BGC*	Output: nonrefresh/bus grant common
13	BGC*	Output: bus grant common (any bus master (except 68010))
14	EXP0BG*	Output: expansion board 0 bus grant
15	EXP1BG*	Output: expansion board 1 bus grant
16	EXP2BG*	Output: expansion board 2 bus grant
17	DKBG*	Output: disk drive bus grant
18	EXP3BG*	Output: expansion board 3 bus grant
19	RFBG*	Output: refresh bus grant
20	VCO	Voltage-controlled oscillator: +5v

NOTATION

XX Boolean AND
* Negation or active low
:= Register output latched clock
+ Boolean OR

EQUATIONS FOR BUS GRANT

DKBG := (DKRQ X ENRAS* X BGACK* X DKRQ*) + EXP3BG X BGACK)

RFBG := (RFRQ X ENRAS* X BGACK* X DKRQ* X EXP3RQ*)
+ (RFBG X BGACK)

EXP2BG := (EXP2RQ X ENRAS* X BGACK* X DKRQ* X EXP3RQ* X RFRQ*)
+ (EXP2BG X BGACK)

EXP1BG := (EXP1RQ X ENRAS* X BGACK* X DKRQ* X EXP3RQ* X RFRQ*
X EXP2RQ*) + (EXP1BG X BGACK)

EXP0BG := (EXP0RQ X ENRAS* X BGACK* X DKRQ* X EXP3RQ* X RFRQ* X
EXP2RQ* X EXP1RQ*) + (EXP0BG X BGACK)

The six preceding logic equations describe the input conditions that produce a DMA bus grant in response to a request from any one of the six devices that requests the bus. The devices are named by the output expression. The equations are listed in order of priority: DKRQ (disk request) is the highest priority; EXP0 (expansion board 0) is the lowest. The 68010 does not appear in these equations, because it receives the bus only when no DMA device is requesting the bus. To the right of the equals sign in each logic equation are four terms in the following form:

[bus grant] = [bus request] X [bus not in use] X [priority term]
+ [latch term]

The first term is the bus request (RFRQ, EXP3RQ, DKRQ, etc.). This term is ANDed with ENRAS* and BGACK*, which form the "bus not in use" term. The result is that, if a bus cycle is in process when a request is made, the bus grant is not issued until the current cycle is completed.

The third term is the priority term. In the equation for EXP3BG, the priority term is DKRQ*, because disk request has a higher priority than expansion board 3. Thus the bus is not granted to expansion board 3 if a refresh request is pending. Each equation has a priority term that names all the devices of higher priority. The first equation for DKBG has no priority term, because there is no device of higher priority. The last equation for expansion board 0 has a priority term that names all devices that may request the bus except itself, since it is the lowest priority. Thus the bus is not granted for a given line if any one of those above is pending.

The fourth term is the latch term, which contains the output of the expression ANDed with bus grant acknowledge. When a bus request is granted, bus grant acknowledge keeps the bus grant active after the bus request is removed. The grant is removed when bus grant acknowledge is removed.

PAL Equations

Equation for Bus Grant Common

$$BGC := (RFRQ + EXP3DRQ + DKRQ + EXP2RQ + EXP1RQ + EXP0RQ) \times (ENRAS^* \times BGACK^*) + BGC \times BGACK$$

$$[\text{bus grant common}] = [\text{any DMA request}] \times [\text{bus not in use}] + [\text{latch}]$$

This equation has the four parts shown above. The first part of this equation contains all the possible DMA devices that could request the bus ANDed with the "bus not in use" term, enable row address strobe, and bus grant acknowledge. Thus, when any DMA device requests the bus, BGC is asserted as soon as the cycle being executed is completed. Completion of the cycle is indicated when ENRAS* and BGACK* are not asserted.

The third term is a latch term consisting of the function output, BGC, ANDed with BGACK. Once the BGC is asserted, it remains asserted as long as the bus grant acknowledge is asserted, and it is deasserted when bus grant acknowledge is deasserted.

Equation for Nonrefresh Bus Grant Common

$$NRFBGC := (EXP3RQ + DKRQ + EXP2RQ + EXP1RQ + EXP0RQ) \times (ENRAS^* \times BGACK^* \times RFQR^*) + (NRFBGC \times BGACK)$$

This nonrefresh bus grant is similar to bus grant common. It becomes active at the end of the current cycle when any DMA device, except refresh, requests the bus.

The last term is again a latch term to keep the bus grant active while the acknowledge is active after the original request becomes inactive.

Disk Interface: PAL 16R4A (Sheet 2: D-6)

Pin Number	Mnemonic	Description
1	1PCK+	Input: processor clock
2	RD*	Input: read--indicates 68010 or DMA device is reading memory or an I/O device
3	WR*	Input: write--indicates 68010 or DMA device is writing to memory or an I/O device
4	DMAR/W*	Input: direct memory access read/write--high indicates RAM memory is being read; low indicates RAM memory is being written
5	FDDRQL	Input: floppy disk drive data request--latched data from floppy disk controller pin 38 DRQ (data request); indicates that the floppy disk controller data register contains assembled data when a sector of the disk is being read or that it is empty during a sector write operation
6	HDBCS*	Input: hard disk buffer chip select--connected to pin 1 of hard disk controller; active low used to enable reading or writing data from the bus interface when controller data buffer is ready to transfer a byte
7	FDCS*	Input: floppy disk chip select--asserted when the 68010 is writing or reading the floppy disk controller data register
8	HDRE*	Input: hard disk read--asserted when the hard disk controller is reading a byte from the bus interface unit during a Sector Write command or when the 68010 is reading data from the disk controller data register; connected to the hard disk controller pin 6

PAL Equations

Pin Number	Mnemonic	Description
9	HDWE*	Input: hard disk write--asserted when the hard disk controller is writing a byte to the bus interface unit during a Sector Write command or when the 68010 is writing data from the disk controller data register; connected to the hard disk controller pin 7
10	GND	Ground
11	OE	Output enable: connected low through a 330-ohm resistor to ground
12	FDRE*	Output: floppy disk read--connected to the RE pin 4 of the floppy disk controller
13	FDWE*	Output: floppy disk write--connected to the WE pin 2 of the floppy disk controller
14	EDTFER*	Output: floppy disk transfer--not connected outside of PAL used by rest of PAL logic to produce floppy disk read and write on pins 12 and 13 described above
15	QB*	Output: latch B output--not connected outside PAL chip used internally to latch status of EDTFER
16	QC*	Output: latched value of QB--not connected outside of PAL
17	QD*	Output: latched value of QC--not connected outside of PAL
18	TFER*	Output: transfer request--goes to disk DMA bus interface unit; initiates transfer of data from disk controller to bus interface unit and generates a disk bus request
19		Output: not used
20	VCC	+5 volts

LOGIC EQUATIONS
$$\text{EDTFER} := (\text{EDDRQL} \times \text{EDTFER}^*) + (\text{EDTFER} \times \text{QD}^*)$$
$$\text{QB} := \text{EDTFER}$$
$$\text{QC} := \text{QB}$$
$$\text{QD} := \text{QC}$$
$$\text{FDRE} := (\text{EDCS} \times \text{RD}) + (\text{EDTFER} \times \text{DMARW})$$
$$\text{FDWE} := (\text{EDCS} \times \text{WR}) + (\text{EDTFER} \times \text{DMARW}^*)$$
$$\begin{aligned} \text{TFER} := & (\text{QD} \times \text{DMARW}^*) + (\text{QD}^* \times \text{DMARW}) + \text{QB} + (\text{HBCS} \times \text{HDRE}) \\ & + (\text{HBCS} \times \text{HDWE}) \end{aligned}$$

The transfer request (TFER) is asserted when the hard disk controller or the floppy disk controller is ready to transfer a byte to or from its data register to or from the disk bus interface unit buffers. On every other assertion of TFER, a disk DMA bus request is issued by the interface unit.

PAL Equations

MMU and Bus Error: PAL 16L8A (Sheet 2: C-6)

Pin Number	Mnemonic	Description
1	PA22	Input
2	KADDR	Input: kernal access address, A19 A20, and A21 all low
3	SUP+	Input: 68010 in supervisor mode
4	BGC*	Input: bus grant common
5	LPS0*	Input: latched page status bit 0
6	LPS1*	Input: latched page status bit 1
7	R/W*	Input: high = read; low = write
8	LWE+	Input: latched page status bit write enable
9	SPA23	Input: highest address bit
10	GND	Ground
11	T90	Input
12	CASDIS*	Output
13	IODTACK*	Input
14	PAS*	Input
15	BERREN	Output: bus error enable
16	PGF*	Output: page fault
17	MMUERR*	Output: memory management unit error
18	UIE*	Output: user access to address outside memory
19	PPS0	Output: updated processor page status bit 0
20	VCC	+5 volts

Memory Management Unit Error Equation

$$\begin{aligned} \text{MMUERR} = & \text{BGC}^* \text{ X } \text{PA22}^* \text{ X } \text{SPA23}^* \text{ X } \text{LPS0}^* \text{ X } \text{LPS1}^* \\ & + \text{BGC} \text{ X } \text{LPS0}^* \text{ X } \text{LPS1}^* \\ & + \text{BGC}^* \text{ X } \text{SUPV}^* \text{ X } \text{SPA23}^* \text{ X } \text{PA22}^* \text{ X } \text{KADDR} \\ & + \text{BGC}^* \text{ X } \text{SUPV}^* \text{ X } \text{PA23}^* \text{ X } \text{PA22}^* \text{ X } \text{RW} \text{ X } \text{LWE}^* \end{aligned}$$

This equation is the logical ORing of four terms, each of which causes a memory management error.

In the first term, BGC*, PA22*, and SPA23* all high indicate a user access to RAM memory. LPS0* and LPS1* both high indicate that the access is to a page that has been designated not physically present.

In the second term, BGC high indicates a DMA access, and LPS0* and LPS1* indicate access is to a page not physically present.

In the third term, SUPV* indicates a user access, 68010 not in supervisory mode, and KADDR indicates the access is to the kernel.

In the fourth term, LWE* indicates the access is to a page not write enabled, and WE* indicates a write cycle.

The four conditions that generate a memory management error are summarized in the following table:

- o Processor access to a page not present
- o DMA access to a page not present
- o User access to the kernel
- o User attempt to write to a page not write enabled

MMUERR is used on sheet 6 to generate a level 7 interrupt.

Page Fault Equation

$$\text{PGF} = \text{BGC}^* \times \text{PA22} \times \text{SPA23}^* \times \text{LPS0}^* \times \text{LPS1}^* \\ + (\text{BGC} \times \text{LPS0}^* \times \text{LPS1}^*)$$

Page fault is the ORing of two terms. In the first, BGC* indicates a 68010 access, and LPS0* and LPS1 indicate access is to a page not present. In the second, BGC indicates a DMA access. Thus page fault occurs when either the 68010 or a DMA device tries to access a page not present.

User Nonmemory Location Error Equation

$$\text{UIE} = (\text{BGC}^* \times \text{SUPV}^* \times \text{ENRAS}^* \times \text{PA22}) + (\text{BGC}^* \times \text{SUPV}^* \times \text{ENRAS}^*)$$

In this equation, SUPV* indicates a user access; PA22 and ENRAS* indicate that the access is to a nonmemory location.

PAL Equations

Bus Error Enable Equation

BERREN= BGC* X PA22* X SPA23* X LPS0* X LPS1* X T90 X PAS
+ BGC* X SUPV* X SPA23* X PA22* X KADDR X T90 X PAS
+ BGC* X SUPV* X SPA23* X PA22* X RW X LWE* X T90
+ BGC* X SUPV* X SPA23* X PA22 X IODTACK
+ BGC* X SUPV* X SPA23* X DTACK

This equation is the ORing of five terms. The condition to assert each term is:

- o User access to page not present
- o User access to kernel
- o User access to page not write enabled
- o User access to address not in memory
- o User access to address not in memory

BERREN is ANDed with EE* (the error enable bit) and connected to BERR- pin 22 of the 68010.

Column Address Disable Strobe Equation

CASDIS = BGC* X PA22* X SPA23* X LPS0* X LPS1* X RW
+ BGC X LPS0* X LPS1* X RW
+ BGC* X SUPV* X SPA23* X PA22* X KADDR X RW
+ BGC* X SUPV* X SPA23* X PA22* X RW X LWE* X RW

The column disable bit prevents writing to RAM memory during a memory management unit error. Thus the terms of these equations contain the same conditions that generate the MMUERR ANDed with the RW write bit.

Page Status Bit 0 Equation

PPS0 = RW* X LPS1* X LPS0 X MMUERR*
+ RW* X LPS1 X LPS0* X MMUERR*
+ LPS0* X MMUERR

This equation lists the following three conditions for setting bit 0 of page status to 1:

- o Writing to a page that is present but has never been written to, when there is no MMUERR

- o Writing to a page that is present and has been read but not previously written to, when there is no MMUERR
- o A MMUERR exists and PS0 was previously written to, when there is no MMUERR
- o A MMUERR exists and PS0 was previously 0.

PAL Equations

Hard Disk Data Separator: PAL 16R4 (Sheet 26)

Pin Number	Mnemonic	Description
1	MUXCLK*	Input clock for multiplex clock output
2	PLLCLK	Output of VCO
3	DATA0	Data and clock from drive 0
4	DATA1	Grounded
5	DDRIVE0*	Grounded
6	HDRGATE	High when disk controller is inspecting data
7	PCLK*	10 MHz
8	TEST	Grounded
9	REF	Grounded
10	GND	
11	OE*	Grounded
12	RCLK	1/2 PLL
13	DCLK	No external connection
14	FFA*	No external connection
15	OSCENB*	Enables VCO
16	FFB*	No external connection
17	FFC*	No external connection
18	CLR*	Clears pullup/pulldown flipflops
19	MUX*	Multiplex clock output
20	VCC	

Equations

FFA : = HDRGATE

FFB := FFA

FFC := FFB

OSCENB := HDRGATE* FFC* + HDRGATE X FFC

CLR = HDRGATE* X FFC + HDRGATE X FFC* + OSCENB*

DCLK* = PLLCLK X RCLK + PLLCLK* X DCLK* + RCLK X DCLK* + TEST

$$RCLK^* = PLLCLK^* \times DCLK^* + PLLCLK \times RCLK^* + DCLK^* \times RCLK^*$$

$$MUX = \begin{matrix} HDRGATE \times DATA0^* \times DDRIVE0 & + & HDRGATE \times DATA1^* \\ & \times & DDRIVE0^* & + & HDRGATE^* \times PCLK^* \end{matrix}$$

If HDRGATE is high, MUX pin 19 outputs drive 0 data coming in on pin 3. If HDRGATE is low, MUX outputs PCK* coming in on pin 7.

When HDRGATE is high, PLLK is phase-locked to DATA0 at pin 3 at twice the frequency. DATA0 is 5 MHz and PLL is 10 MHz.

When HDRGATE is low, PLLK is 10 MHz, phase locked to PCK* at pin 7.

RCLK is always half the frequency of PLLCLK.



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B Mnemonics

<u>Mnemonic</u>	<u>Description</u>
A	
A1-A23	System address bits
ABUS	System address bus
ADX	Address
ARB	Bus arbitor
AUTO FEEDXT	Automatic line feed
B	
BCS	Buffer chip select
BERR	Bus error
BERREN	Bus error enable
BGACK	Bus grant acknowledge
BGC	Bus grant common
BGCAK	Bus grant common acknowledge
BM WINDOW	Bit map window
BMACK	Bit map acknowledge
BMCAS	Bit map column address strobe
BMRAS	Bit map row address strobe
BMR/W	Bit map read/write
BMSEL	Bit map select
BP	Bad parity
BRABUS 0-7	Bit map RAM address bus
BSR0RD	Bus status register 0 read
C	
CAS	Column address strobe
CASDIS	Column address strobe disable
CASEN	Column address strobe enable
CCK	Character clock
CD	Carrier detect
CLR 60HZ INT	Clear 60-Hz interrupt
CLRREFADD	Clear refresh address
CO	Carryout
COMMOSC	Communications oscillator
CPU	Central processing unit
CS	Chip select
CSR	Clear status register
CTS	Clear to send

Mnemonics

D

D0-D15	System data bits
DADDWR	Direct memory access address counter write
DATAIN	Data in
DBLDEN	Double density
DBUS	System data bus
DCNTCS	Direct memory access word counter chip select
DCS	Disk controller select
DD	Disk data bus
DDBUS 0-7	Disk data bus 0-7
DDRIVE0	Disk drive 0
DEFAULT	Data fault
DIALER EN	Dialer enable
DIALER TXD	Dialer transmit data
DINDEX	Disk index pulses
DISPEN	Display enable
DKBG	Disk bus grant
DKBGA	Disk bus grant acknowledge
DKRQ	Disk bus request
DMA	Direct memory access
DMAEN	Direct memory access enable
DMAR	Direct memory access read
DMAR/W	Direct memory access read/write
D/N CONNECT 1	Dial network connected to line 1
DREADY	Drive ready
DRQ	Data request
DRUN	Data run
DSCOMPL	Disk seek complete
DSR	Data set ready
DT DET	Dial tone detect
DTACK	Data transfer acknowledge
DTRK 0	Disk track 0

E

EE	Error enable
EN	Enable
ENCAS	Enable column address strobe
ENRAS	Enable row address strobe
EXP0-3BG	Expansion board 0-3 bus grant
EXP0-3RQ	Expansion board 0-3 request

F

FC	Function code
FDCS	Floppy disk chip select
FDDRIVE0	Floppy disk drive 0
FDDRQ	Floppy disk data request
FDDRQL	Floppy disk data request latched
FDINDEX	Floppy disk index
FDINTRQ	Floppy disk interrupt request
FDMOTOR	Floppy disk motor enable
FDPRESENT	Floppy disk present
FDRD	Floppy disk read
FDRE	Floppy disk read enable
FDREADY	Floppy disk ready
FDRST	Floppy disk reset
FDTRACK 0	Floppy disk track 0
FDWE	Floppy disk write enable
FDWPRT	Floppy disk write protect
FF	Flipflop
FWR	Fast write

G

GCRRW	General control register write
GND	Ground
GSR	General status register
GSRRD	General status register read

H

HAL	Hard array of logic
HDBCS	Hard disk buffer chip select
HDBRDY	Hard disk buffer ready
HDCS	Hard disk chip select
HDCTRLWR	Hard disk controller write
HDINTRQ	Hard disk interrupt request
HDL	Head load
HDRE	Hard disk read enable
HDRST	Hard disk reset
HDSEL0-2	Head select bits 0-2
HDSETRELAY	Handset relay
HDWDATA	Hard disk write data
HDWE	Hard disk write enable
HSYNC	Horizontal synchronization

Mnemonics

I

ID	Identify
IDMAR/W	Identify DMA read/write operation
INIT	Centronics reset and initialize control signal
INT	Interrupt
INTA	Interrupt acknowledge
INTRQ	Interrupt request
I/O DTACK	I/O data transfer acknowledge
I/OEN	I/O enable
I/ORQ	I/O request
IPL	Interrupt priority level

K

KADDR	Kernel address
KBEN	Keyboard enable
KBINT	Keyboard interrupt
KBRST	Keyboard reset
KBRXD	Keyboard receive data
KBTXD	Keyboard transmit data

L

L1 A-LEAD	Line 1 A-lead
L1 HOLD	Line 1 hold
L1 MODEM	Line 1 modem
L1 RING	Line 1 ring
L2 A-LEAD	Line 2 A-lead
L2 HOLD	Line 2 hold
L2 MODEM	Line 2 modem
L2 RING	Line 2 ring
LA	Latched address
LA BUS	Local address bus
LBERR	Latched bus error
LCAS	Lower column address strobe
LDS	Lower data strobe
LINE SEL2	Line select 2
LMA	Latched map address
LMUXPAR	Lower multiplexed parity
LPACK	Line printer acknowledge
LPARIN	Lower parity interrupt
LPAROUT	Low parity output

L (continued)

LPBUSY	Line printer busy
LPDATAWR	Line printer data write
LPINT	Line printer interrupt
LPNOPAPER	Line printer out of paper
LPS	Latched page status
LPSELECT	Line printer select
LPSTATUSRD	Line printer status read
LPSTROBE	Line printer strobe
LWE	Latched write enable

M

MA	Mapped address
MA BUS	Mapped address bus
MCK	Modem clock
MCKSEL	Modem clock select
MEMEN	Memory enable
MEF	Modified frequency modulation
MMU	Memory management unit
MMUERR	Memory management unit error
MMUWR	Memory management unit write
MMUWREN	Memory management unit write/read enable
MMUWREND	Memory management unit write/read enable data
MODEM CK SEL	Modem clock select
MODEM RXCK	Modem receive clock
MODEM RXD	Modem receive data
MODEM TXCK	Modem transmit clock
MODEM TXD	Modem transmit data
MODEMCS	Modem chip select
MOSEN	Processor data transceiver enable
MPU	Microprocessing unit
MRAEN	Map RAM enable
MRAMEN	Map RAM enable
MREG WR	Miscellaneous control register write
MSG WAIT	Message waiting
MW	Memory write

N

NMI	Nonmaskable interrupt
NPC	Nonprocessor cycle
NREBGC	Nonrefresh bus grant common

Mnemonics

O

OSCENB Oscillator enable

P, Q

PA BUS Processor address bus
PAL Programmable array of logic
PAS Processor address strobe
PCK Processor clock
PCLK Processor clock
PD Pumpdown
PD BUS Processor data bus
PF Page fault
PIE Parity interrupt enable
PRD1-8 Line printer data bits

R

RAMEN RAM enable
RAS Row address strobe
RD Read
REBG Refresh bus grant
RERQ Refresh bus request
ROMEN Read only memory enable
RTCALE Realtime clock address latch enable
RTCD0-4 Realtime data bits
RTCLE Realtime clock latch enable
RTCR/W Realtime clock read/write
R/W Read/write

S

SUPV Supervisory mode

T

T30-T120 Memory timing delay outputs in nanoseconds
TFER Transfer request
TPD0-7 Serial controller data bus

U, V

UCAS	Upper column address strobe
UDS	Upper data strobe
UIE	User interrupt error
U/OERR	Disk DMA underrun or overrun error

W

WE	Write enable
WR	Write

X, Y, Z

XI/O EN	Expansion I/O enable
XPERR	Expansion parity error

C Expansion Memory Locations

This appendix is a table listing the possible memory configurations for the UNIX PC.

The columns of the table are labeled as follows:

- o Total System Memory - This is the total amount of Random Access memory (RAM) on the machine including on-board (CPU) memory and expansion memory.
- o CPU On-Board Memory - This is the amount of RAM on the UNIX PC main sytem board.
- o Expansion Memory Slot 1 - This is the first UNIX PC expansion slot. Facing the rear of the machine, it is located on the left side as shown in Figure 1.
- o Expansion Memory Slot 2 - This is the second UNIX PC expansion slot. Facing the rear of the machine, it is the middle slot as shown in Figure 1.
- o Expansion Memory Slot 3 - This is the third UNIX PC expansion slot. Facing the rear of the machine, it is located on the right as shown in Figure 1.

Expansion Memory Locations

The table also uses the following mnemonics:

<u>MNEMONIC</u>	<u>MEANING</u>
*	Empty slot or I/O card without memory
0.5 CPU	UNIX PC equipped with 0.5MB of on-board RAM
1.0 CPU	UNIX PC equipped with 1.0MB of on-board RAM
2.0 CPU	UNIX PC equipped with 2.0MB of on-board RAM
0.5 RAM	0.5MB RAM Expansion Board
2.0 RAM	2.0MB RAM Expansion Board
0.5 EIA	EIA/RAM Combo Board with 0.5MB of RAM
1.0 EIA	EIA/RAM Combo Board with 1.0MB of RAM
1.5 EIA	EIA/RAM Combo Board with 1.5MB of RAM

How to Use this Table

The table is organized according to the total amount of memory the system will have after installing additional memory cards. The following examples illustrate how to use the table.

1. You have a UNIX PC with 0.5MB of on-board memory and you want to install a 0.5MB memory expansion board, bringing the total memory to 1.0MB. First look in the Total System Memory column for 1.0MB. Then, locate the corresponding amount of on-board memory in the next column, in this case 0.5MB. Next, look at the last three columns. You'll see that you can put your 0.5MB RAM board in expansion slot 1, 2, or 3.
2. If you want to install a second 0.5MB RAM expansion board, bringing your systems total memory to 1.5MB, you would look in the Total System Memory column for 1.5MB. Then, you would look for the same amount of on-board memory, or 0.5MB. Next, you would look at the last three columns to see where you can place the additional expansion card. In this case, the two 0.5MB RAM cards have to be placed in either expansion slots 1 and 2, or in slots 2 and 3. You cannot place them slots 1 and 3.

Expansion Memory Locations

Expansion Memory Locations

TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
0.5 MB	0.5 CPU	*	*	*
1.0 MB	0.5 CPU	0.5 RAM	*	*
		* *	0.5 RAM *	* 0.5 RAM
		0.5 EIA * *	* 0.5 EIA *	* * 0.5 EIA
	1.0 CPU	*	*	*
1.5 MB	0.5 CPU	0.5 RAM *	0.5 RAM 0.5 RAM	* 0.5 RAM
		0.5 EIA *	0.5 RAM 0.5 RAM	* 0.5 EIA
		1.0 EIA * *	* 1.0 EIA *	* * 1.0 EIA
	1.0 CPU	0.5 RAM * *	* 0.5 RAM *	* * 0.5 RAM
		0.5 EIA * *	* 0.5 EIA *	* * 0.5 EIA

Expansion Memory Locations

Expansion Memory Locations (Continued)

TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
2.0 MB	0.5 CPU	0.5 RAM	0.5 RAM	0.5 RAM
		0.5 RAM	0.5 RAM	0.5 EIA
		1.0 EIA *	* 1.0 EIA	0.5 RAM 0.5 RAM
		0.5 EIA 0.5 EIA 1.0 EIA * 1.0 EIA *	1.0 EIA * 0.5 EIA 0.5 EIA * 1.0 EIA	* 1.0 EIA * 1.0 EIA 0.5 EIA 0.5 EIA
		1.5 EIA * *	* 1.5 EIA *	* * 1.5 EIA
	1.0 CPU	0.5 RAM *	0.5 RAM 0.5 RAM	* 0.5 RAM
		0.5 EIA *	0.5 RAM 0.5 RAM	* 0.5 EIA
		1.0 EIA * *	* 1.0 EIA *	* * 1.0 EIA
	2.0 CPU	*	*	*

Expansion Memory Locations

Expansion Memory Locations (Continued)

TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
2.5 MB	0.5 CPU	2.0 RAM * *	* 2.0 RAM *	* * 2.0 RAM
	1.0 CPU	0.5 RAM	0.5 RAM	0.5 RAM
		0.5 RAM	0.5 RAM	0.5 EIA
		1.0 EIA *	* 1.0 EIA	0.5 RAM 0.5 RAM
		0.5 EIA 0.5 EIA 1.0 EIA *	1.0 EIA * 0.5 EIA 0.5 EIA *	* 1.0 EIA * 1.0 EIA 0.5 EIA 0.5 EIA *
		1.0 EIA *	1.0 EIA *	0.5 EIA *
		1.5 EIA * *	1.5 EIA *	1.5 EIA
	2.0 CPU	0.5 RAM * *	* 0.5 RAM *	* * 0.5 RAM
		0.5 EIA * *	* 0.5 EIA *	* * 0.5 EIA

Expansion Memory Locations

Expansion Memory Locations (Continued)

TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
3.0 MB	1.0 CPU	2.0 RAM * *	* 2.0 RAM *	* * 2.0 RAM
	2.0 CPU	0.5 RAM * 0.5 RAM	0.5 RAM 0.5 RAM *	* 0.5 RAM 0.5 RAM
		0.5 RAM 0.5 RAM 0.5 EIA * *	0.5 EIA * 0.5 RAM 0.5 RAM *	* 0.5 EIA * 0.5 EIA *
		1.0 EIA * *	* 1.0 EIA *	* * 1.0 EIA
3.5 MB	2.0 CPU	0.5 RAM	0.5 RAM	0.5 RAM
		0.5 RAM	0.5 RAM	0.5 EIA
		1.0 EIA *	* 1.0 EIA	0.5 RAM 0.5 RAM
		0.5 EIA 0.5 EIA 1.0 EIA * 1.0 EIA *	1.0 EIA * 0.5 EIA 0.5 EIA * 1.0 EIA	* 1.0 EIA * 1.0 EIA 0.5 EIA 0.5 EIA

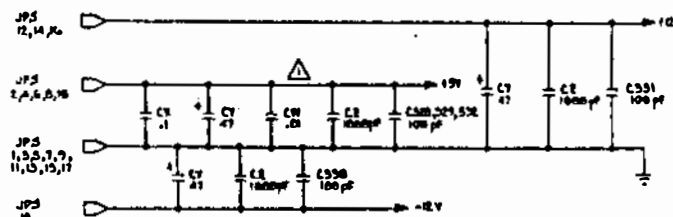
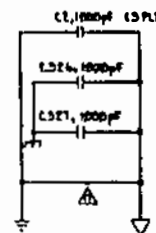
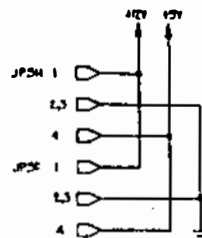
Expansion Memory Locations

Expansion Memory Locations (Continued)

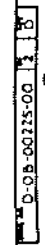
TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
3.5 MB (cont'd)	2.0 CPU (cont'd)	1.5 EIA * *	* 1.5 EIA *	* * 1.5 EIA
4.0 MB	2.0 CPU	2.0 RAM * *	* 2.0 RAM *	* * 2.0 RAM

NOTES: UNLESS OTHERWISE SPECIFIED

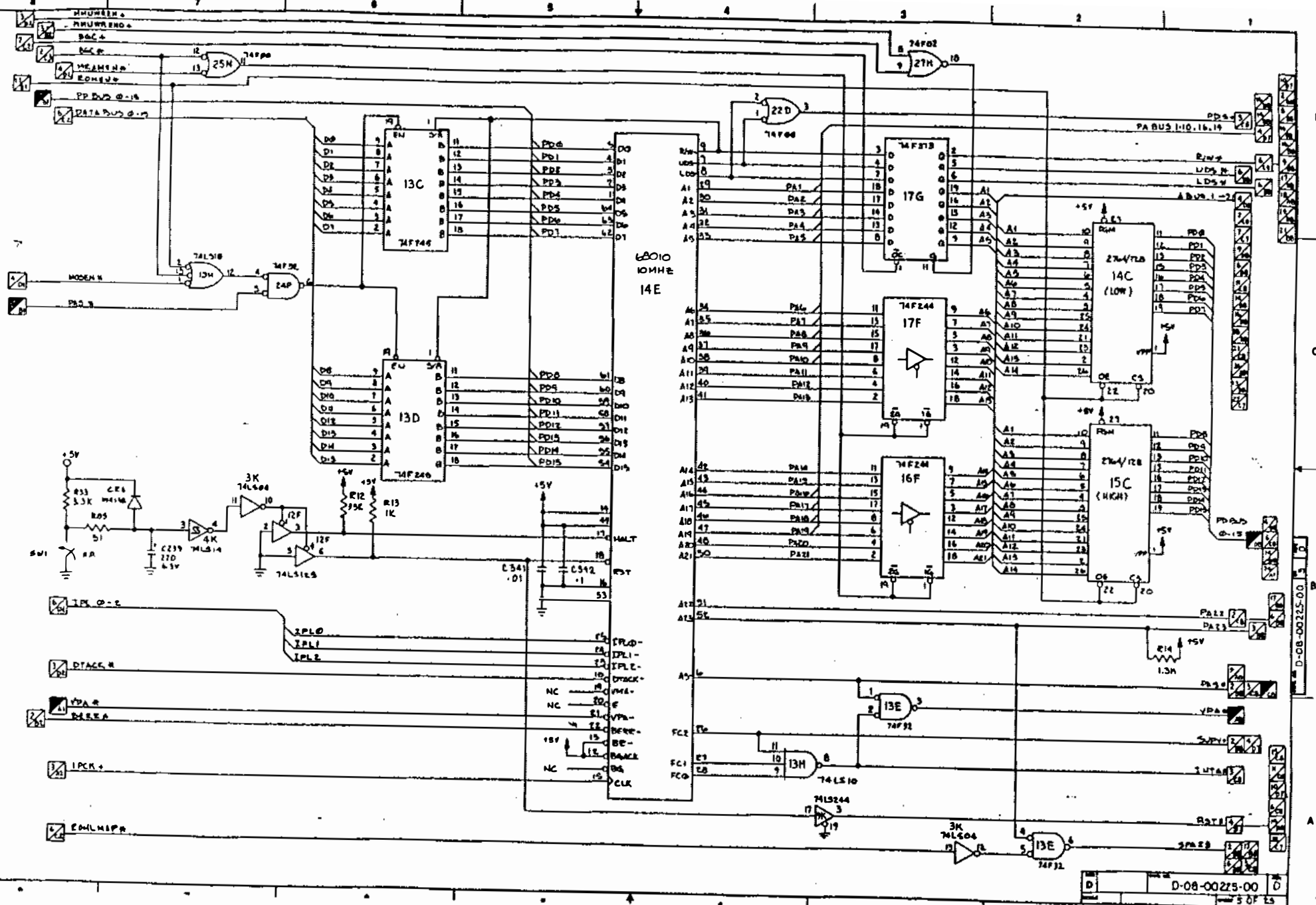
1. ON CAPS ARE USED MEDIA 1 C'S WITH 10 MHE.
2. PM 11 SHOULD CONNECT TO +12V; PM 1 TO -12V.
3. THESE GATES MUST BE IN THE SAME PACKAGE (PROCS 3, 16) (LAYOUT).
4. ALL OUTPUT TRACES ON 74LS159 SHOULD BE AS SHORT AS POSSIBLE. (LAYOUT).
5. SHOULD BE A SHORT TRACE AND NO HIGH FREQUENCY TRACE NEARBY. (LAYOUT).
6. STUFFING OPTIONS: WITH 74LS159 STUFF R94 (NOT R95). C300 SHOULD BE 27P WITH 74LS159 STUFF R95 (NOT R94). C300 SHOULD BE 30P.
7. M95 4750 IS AN ALTERNATE PART.
8. THESE COMPONENTS ARE ONLY TO BE STUFFED WHEN USING CONTROLLERS OTHER THAN M01751.
9. DELETED.
10. DELETED.
11. THESE CAPACITORS SHOULD BE LOCATED NEXT TO T1 AND T2. (LAYOUT).
12. HEAVY TRACE LINES INDICATE 25 MIL TRACES, 50 MIL AIR GAP. (LAYOUT).
13. ALL 15A, 1IN RESISTORS SHOULD BE NON-FLAMMABLE.
14. ALL 1/2W RESISTORS ARE TO BE NON-FLAMMABLE.
15. $\downarrow$ INDICATES ANALOG GROUND.
16. $\frac{1}{2}$ INDICATES DIGITAL GROUND.
17. DIGITAL AND ANALOG GROUND SHOULD ONLY BE CONNECTED AT SUPPLY ORIGIN. (LAYOUT).
18. ALL RELAYS ARE SHOWN AS DE-ACTIVATED.
19. CAPACITORS INDICATED SHOULD BE AS CLOSE TO I.C.'S AS POSSIBLE. (LAYOUT).
20. $\downarrow$ INDICATES USING THE SHORTEST TRACE POSSIBLE BETWEEN THE COMPONENT AND ANALOG GROUND. (LAYOUT).
21. +12V AND -12V TO BE CONNECTED ONLY FROM SUPPLY ORIGIN. (LAYOUT).
22. TRANSISTOR MOUNTED ON MONITOR CASE.
23. ∇ INDICATED ORISSIS GROUND.
24. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.
25. ALL 1W RESISTORS ARE 1/4W.
26. CAPACITOR VALUES ARE IN MICROFARADS.
27. THIS TRACE SHOULD BE AS SHORT AS POSSIBLE. (LAYOUT).
28. R142 TO BE INSTALLED WHEN USING WRITE PRE-COMP.
29. R94-R99 ONLY TO BE INSTALLED WHEN R141 AND/OR R142 ARE NOT INSTALLED.



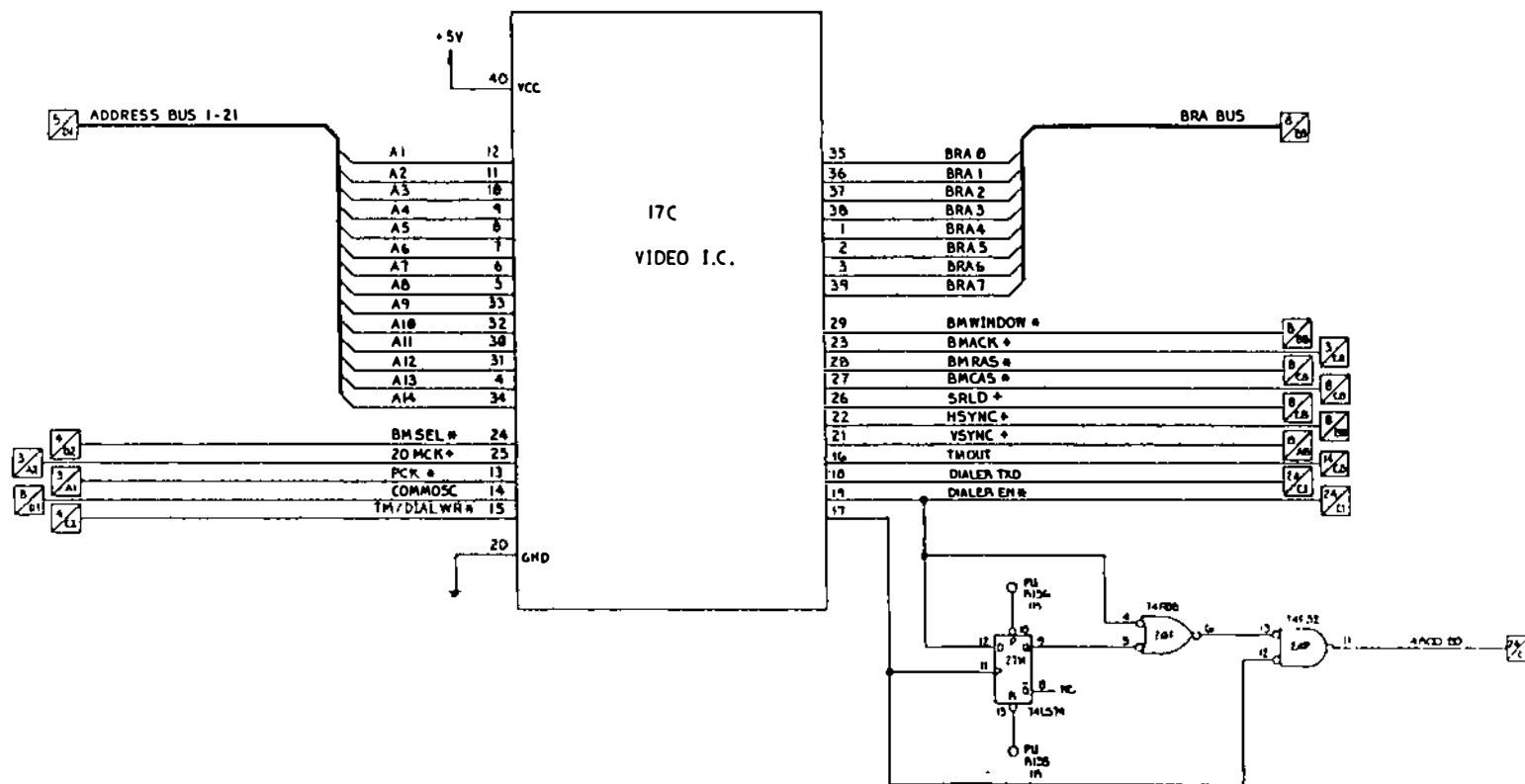
REFERENCE DESIGNATIONS	
USED	NOT USED
C342	C1-33, 41-64, 67-81, 89, 93-101, 104-117, 102, 109-113, 111, 115, 117, 118, 119, 121, 123, 125, 127, 128, 129, 131, 133, 135, 137, 139, 141, 143, 145, 147, 149, 151, 153, 155, 157, 159, 161, 163, 165, 167, 169, 171, 173, 175, 177, 179, 181, 183, 185, 187, 189, 191, 193, 195, 197, 199, 201, 203, 205, 207, 209, 211, 213, 215, 217, 219, 221, 223, 225, 227, 229, 231, 233, 235, 237, 239, 241, 243, 245, 247, 249, 251, 253, 255, 257, 259, 261, 263, 265, 267, 269, 271, 273, 275, 277, 279, 281, 283, 285, 287, 289, 291, 293, 295, 297, 299, 301, 303, 305, 307, 309, 311, 313, 315, 317, 319, 321, 323, 325, 327, 329, 331, 333, 335, 337, 339, 341, 343, 345, 347, 349, 351, 353, 355, 357, 359, 361, 363, 365, 367, 369, 371, 373, 375, 377, 379, 381, 383, 385, 387, 389, 391, 393, 395, 397, 399, 401, 403, 405, 407, 409, 411, 413, 415, 417, 419, 421, 423, 425, 427, 429, 431, 433, 435, 437, 439, 441, 443, 445, 447, 449, 451, 453, 455, 457, 459, 461, 463, 465, 467, 469, 471, 473, 475, 477, 479, 481, 483, 485, 487, 489, 491, 493, 495, 497, 499, 501, 503, 505, 507, 509, 511, 513, 515, 517, 519, 521, 523, 525, 527, 529, 531, 533, 535, 537, 539, 541, 543, 545, 547, 549, 551, 553, 555, 557, 559, 561, 563, 565, 567, 569, 571, 573, 575, 577, 579, 581, 583, 585, 587, 589, 591, 593, 595, 597, 599, 601, 603, 605, 607, 609, 611, 613, 615, 617, 619, 621, 623, 625, 627, 629, 631, 633, 635, 637, 639, 641, 643, 645, 647, 649, 651, 653, 655, 657, 659, 661, 663, 665, 667, 669, 671, 673, 675, 677, 679, 681, 683, 685, 687, 689, 691, 693, 695, 697, 699, 701, 703, 705, 707, 709, 711, 713, 715, 717, 719, 721, 723, 725, 727, 729, 731, 733, 735, 737, 739, 741, 743, 745, 747, 749, 751, 753, 755, 757, 759, 761, 763, 765, 767, 769, 771, 773, 775, 777, 779, 781, 783, 785, 787, 789, 791, 793, 795, 797, 799, 801, 803, 805, 807, 809, 811, 813, 815, 817, 819, 821, 823, 825, 827, 829, 831, 833, 835, 837, 839, 841, 843, 845, 847, 849, 851, 853, 855, 857, 859, 861, 863, 865, 867, 869, 871, 873, 875, 877, 879, 881, 883, 885, 887, 889, 891, 893, 895, 897, 899, 901, 903, 905, 907, 909, 911, 913, 915, 917, 919, 921, 923, 925, 927, 929, 931, 933, 935, 937, 939, 941, 943, 945, 947, 949, 951, 953, 955, 957, 959, 961, 963, 965, 967, 969, 971, 973, 975, 977, 979, 981, 983, 985, 987, 989, 991, 993, 995, 997, 999, 1001, 1003, 1005, 1007, 1009, 1011, 1013, 1015, 1017, 1019, 1021, 1023, 1025, 1027, 1029, 1031, 1033, 1035, 1037, 1039, 1041, 1043, 1045, 1047, 1049, 1051, 1053, 1055, 1057, 1059, 1061, 1063, 1065, 1067, 1069, 1071, 1073, 1075, 1077, 1079, 1081, 1083, 1085, 1087, 1089, 1091, 1093, 1095, 1097, 1099, 1101, 1103, 1105, 1107, 1109, 1111, 1113, 1115, 1117, 1119, 1121, 1123, 1125, 1127, 1129, 1131, 1133, 1135, 1137, 1139, 1141, 1143, 1145, 1147, 1149, 1151, 1153, 1155, 1157, 1159, 1161, 1163, 1165, 1167, 1169, 1171, 1173, 1175, 1177, 1179, 1181, 1183, 1185, 1187, 1189, 1191, 1193, 1195, 1197, 1199, 1201, 1203, 1205, 1207, 1209, 1211, 1213, 1215, 1217, 1219, 1221, 1223, 1225, 1227, 1229, 1231, 1233, 1235, 1237, 1239, 1241, 1243, 1245, 1247, 1249, 1251, 1253, 1255, 1257, 1259, 1261, 1263, 1265, 1267, 1269, 1271, 1273, 1275, 1277, 1279, 1281, 1283, 1285, 1287, 1289, 1291, 1293, 1295, 1297, 1299, 1301, 1303, 1305, 1307, 1309, 1311, 1313, 1315, 1317, 1319, 1321, 1323, 1325, 1327, 1329, 1331, 1333, 1335, 1337, 1339, 1341, 1343, 1345, 1347, 1349, 1351, 1353, 1355, 1357, 1359, 1361, 1363, 1365, 1367, 1369, 1371, 1373, 1375, 1377, 1379, 1381, 1383, 1385, 1387, 1389, 1391, 1393, 1395, 1397, 1399, 1401, 1403, 1405, 1407, 1409, 1411, 1413, 1415, 1417, 1419, 1421, 1423, 1425, 1427, 1429, 1431, 1433, 1435, 1437, 1439, 1441, 1443, 1445, 1447, 1449, 1451, 1453, 1455, 1457, 1459, 1461, 1463, 1465, 1467, 1469, 1471, 1473, 1475, 1477, 1479, 1481, 1483, 1485, 1487, 1489, 1491, 1493, 1495, 1497, 1499, 1501, 1503, 1505, 1507, 1509, 1511, 1513, 1515, 1517, 1519, 1521, 1523, 1525, 1527, 1529, 1531, 1533, 1535, 1537, 1539, 1541, 1543, 1545, 1547, 1549, 1551, 1553, 1555, 1557, 1559, 1561, 1563, 1565, 1567, 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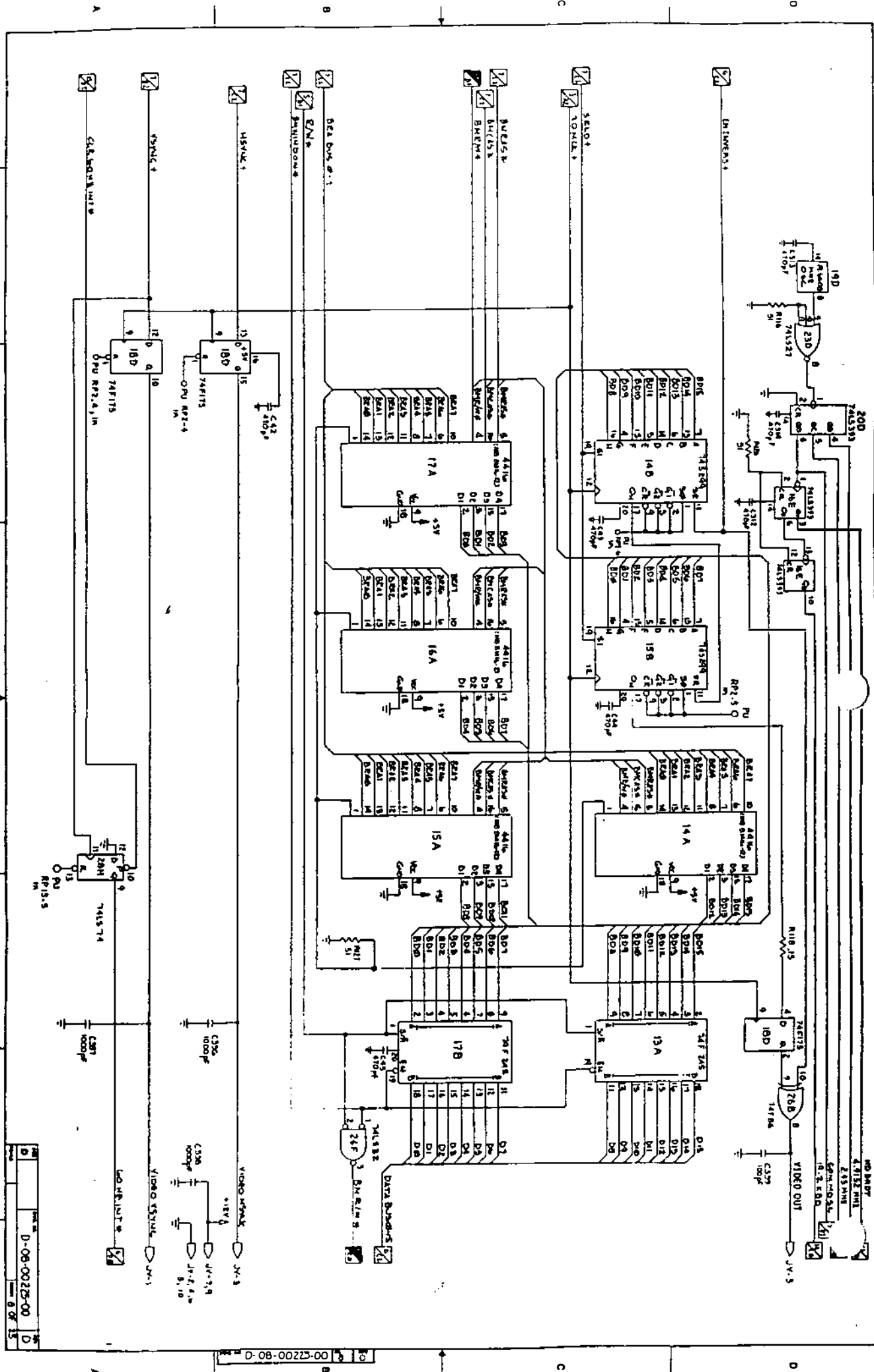






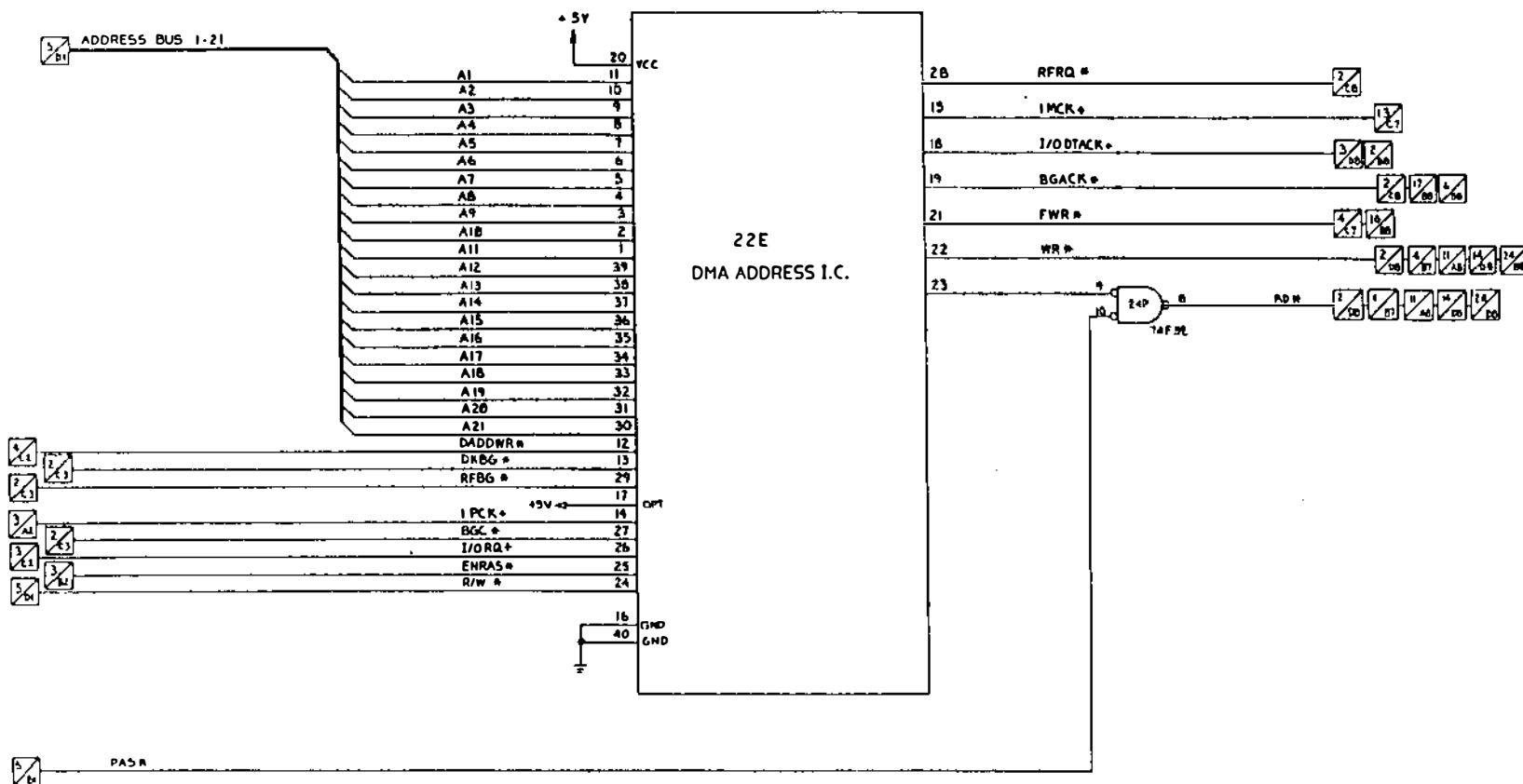


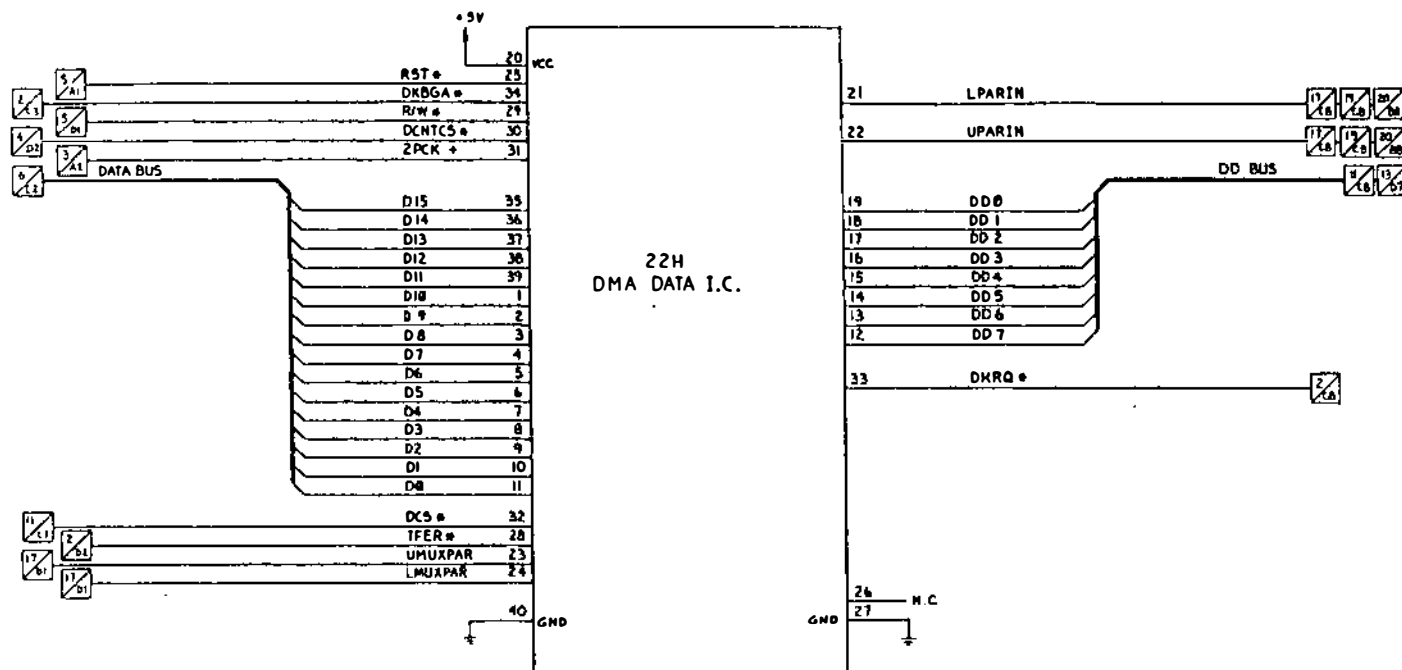


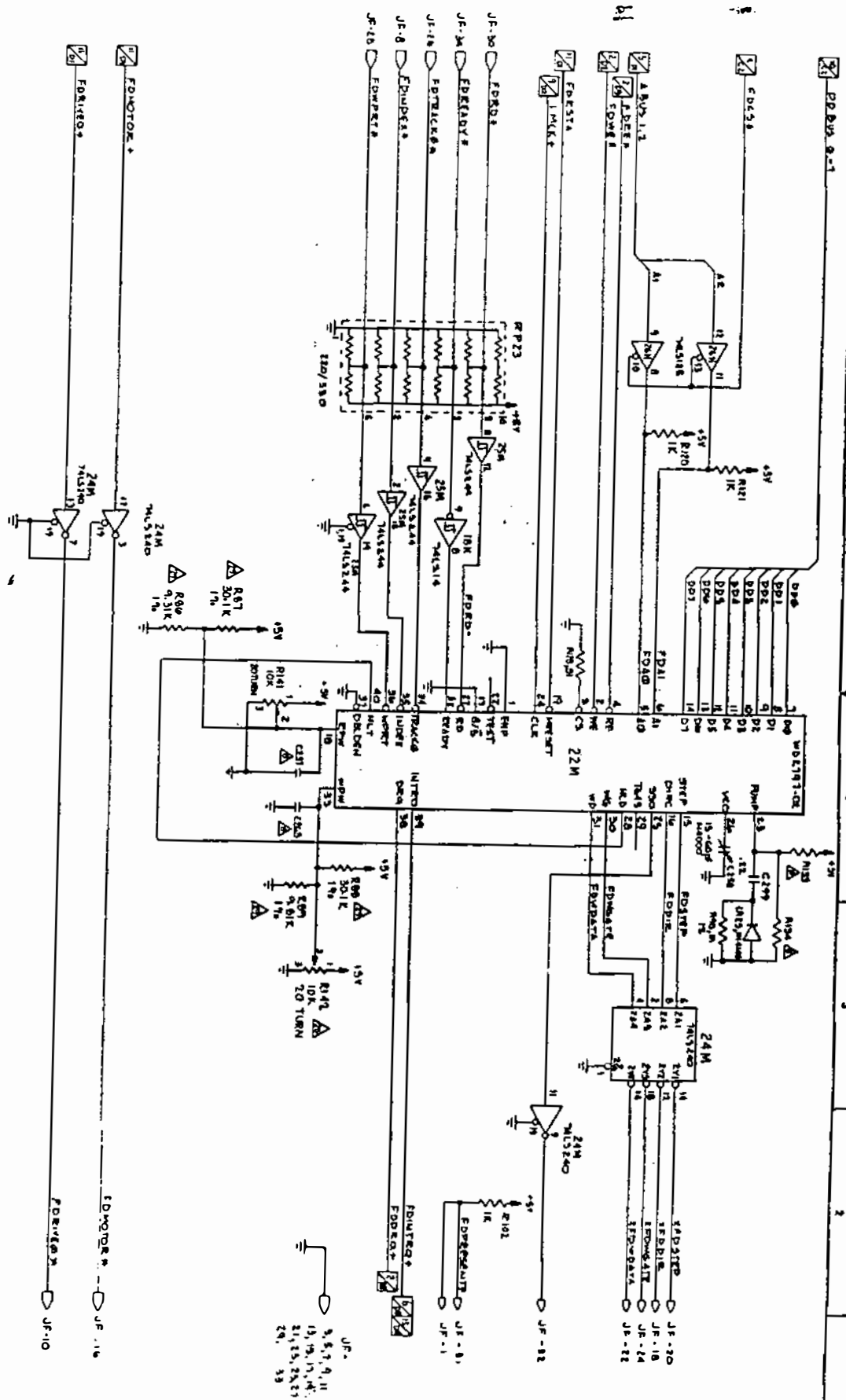


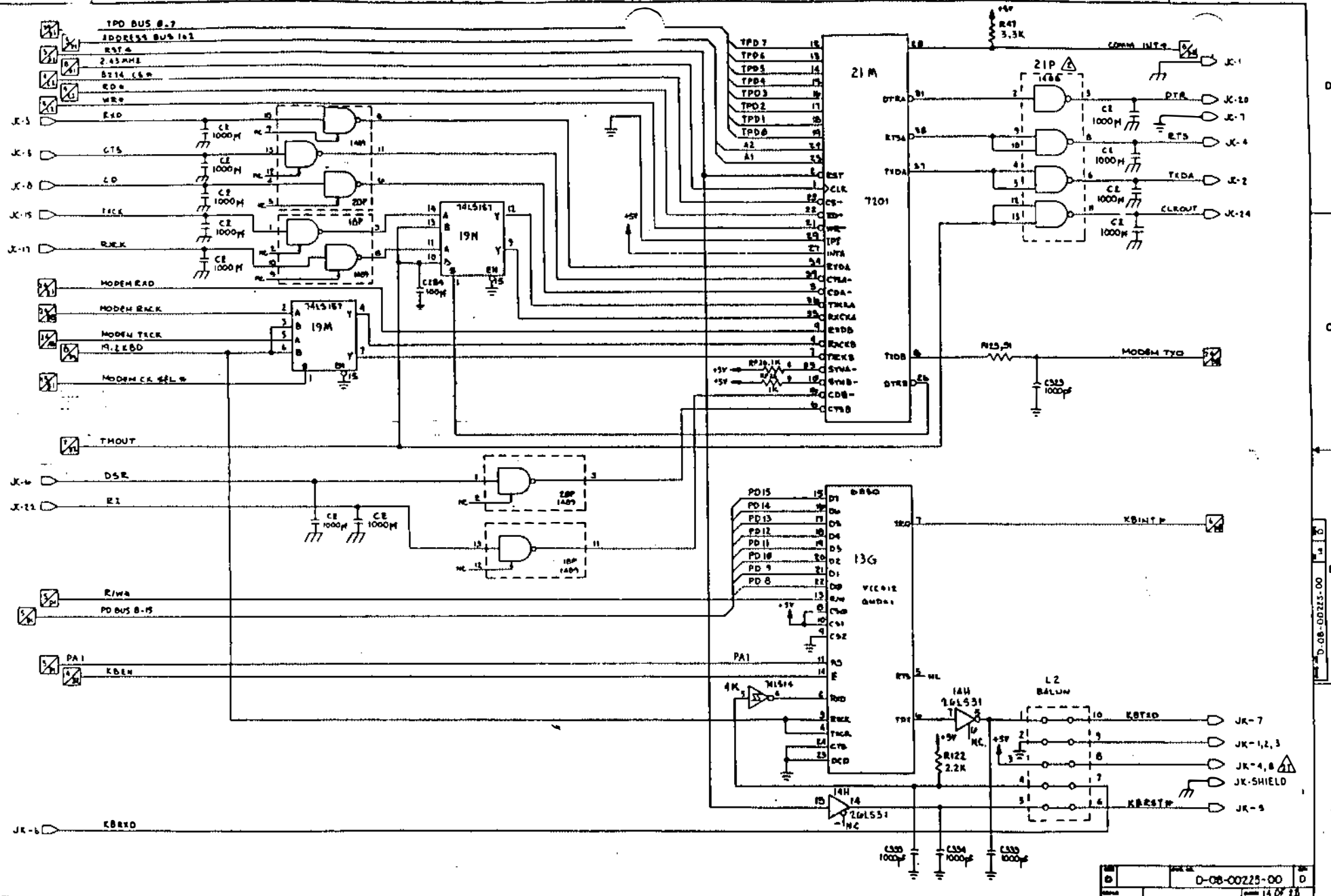
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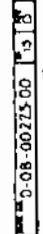
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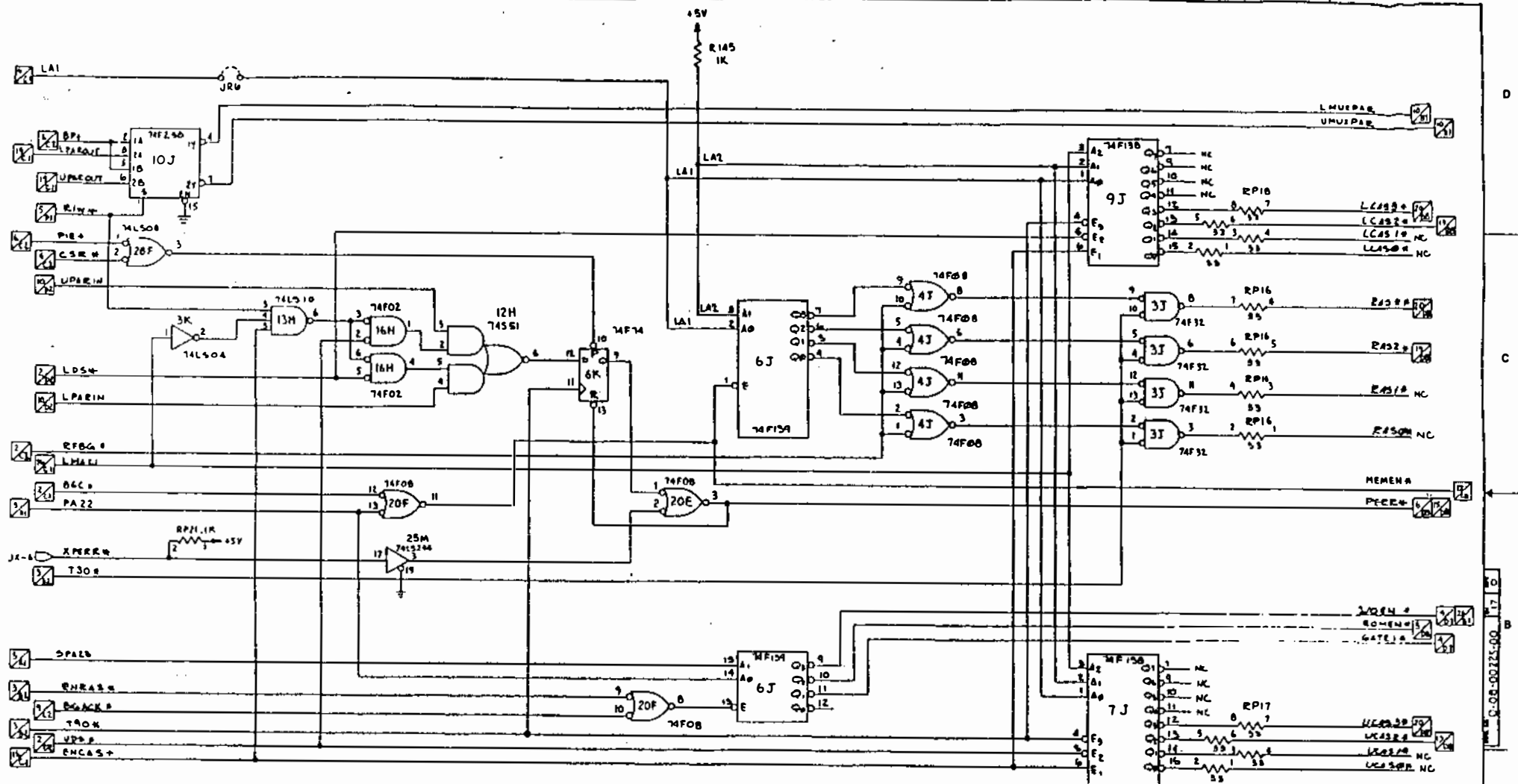


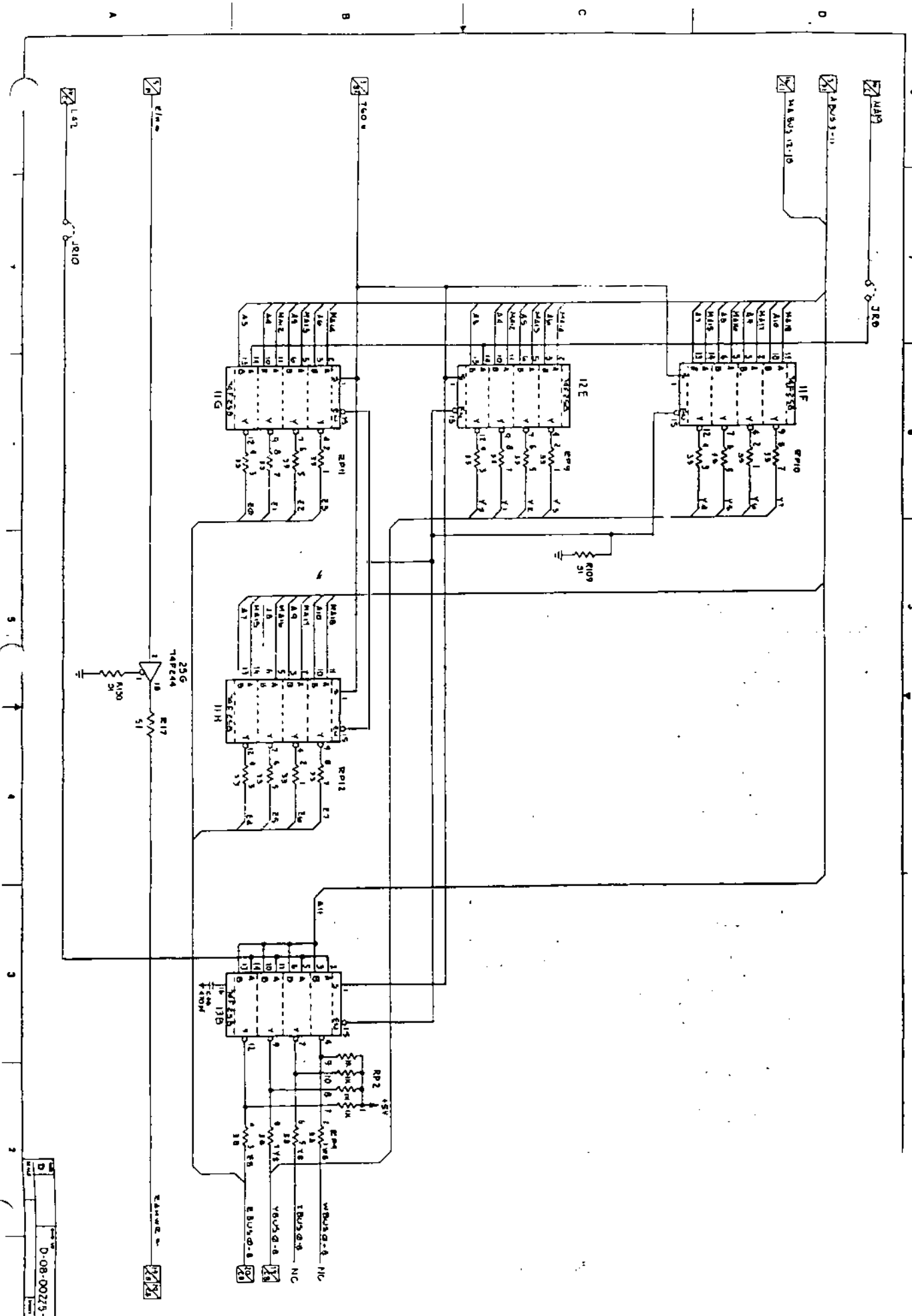


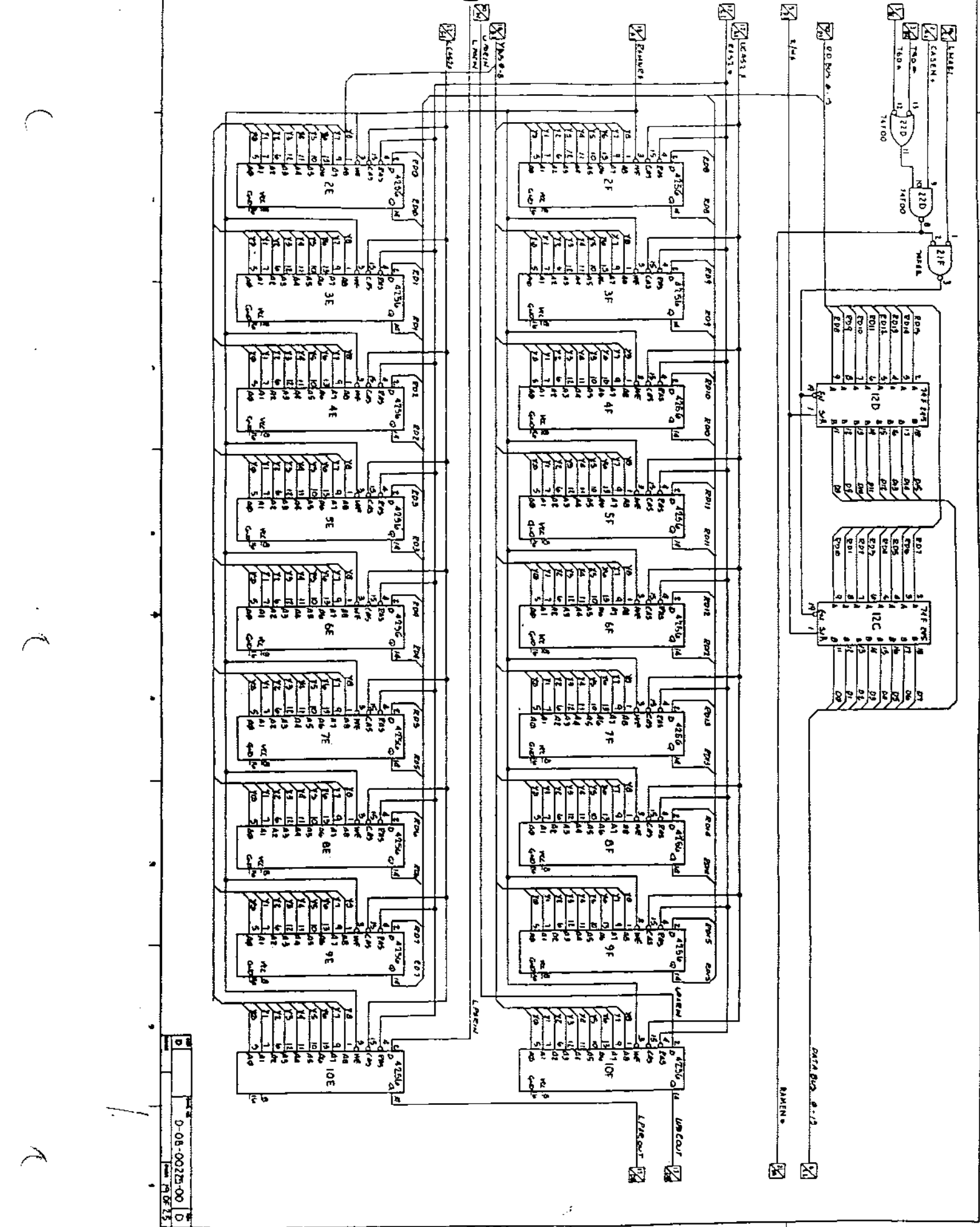


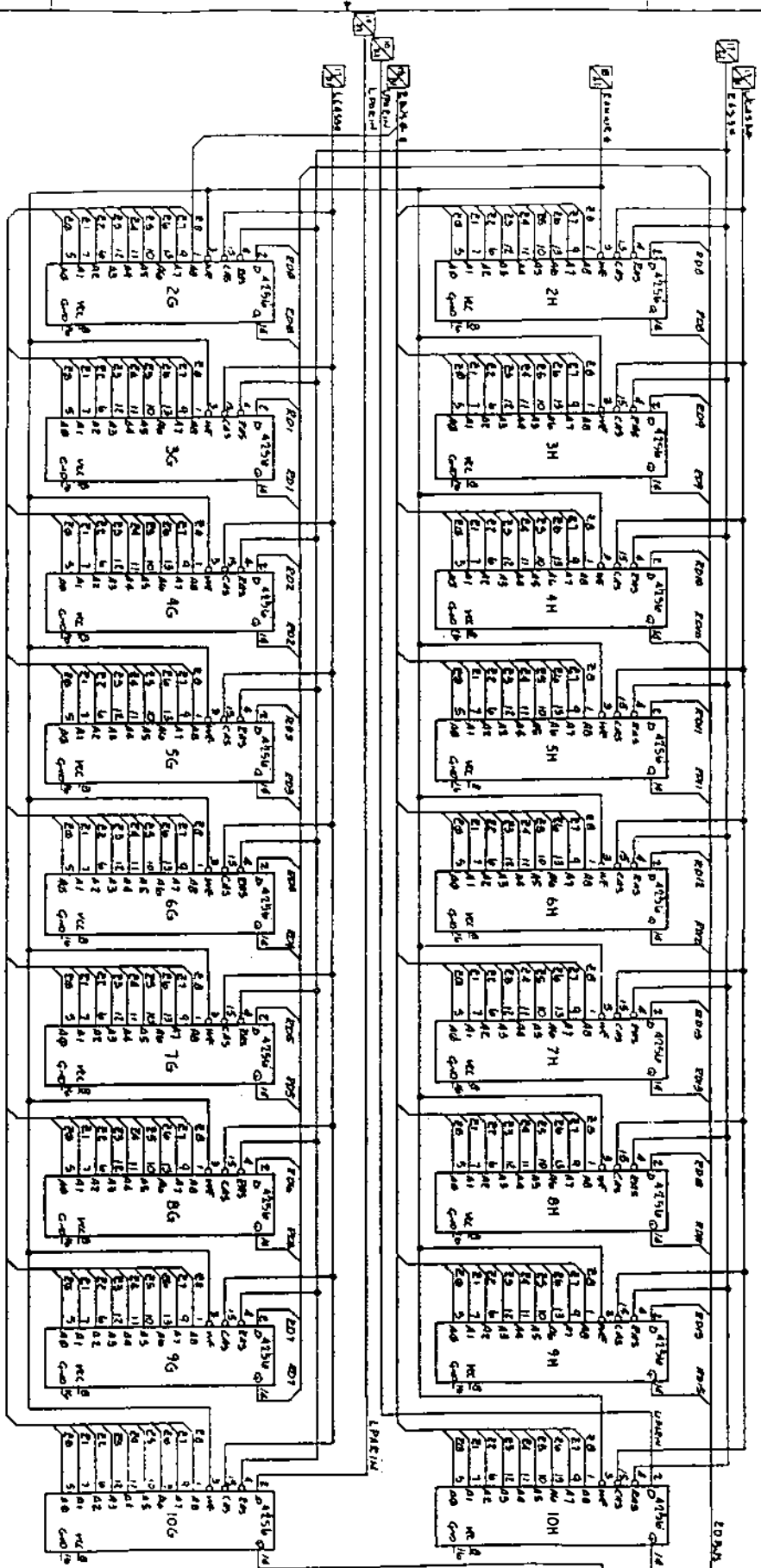






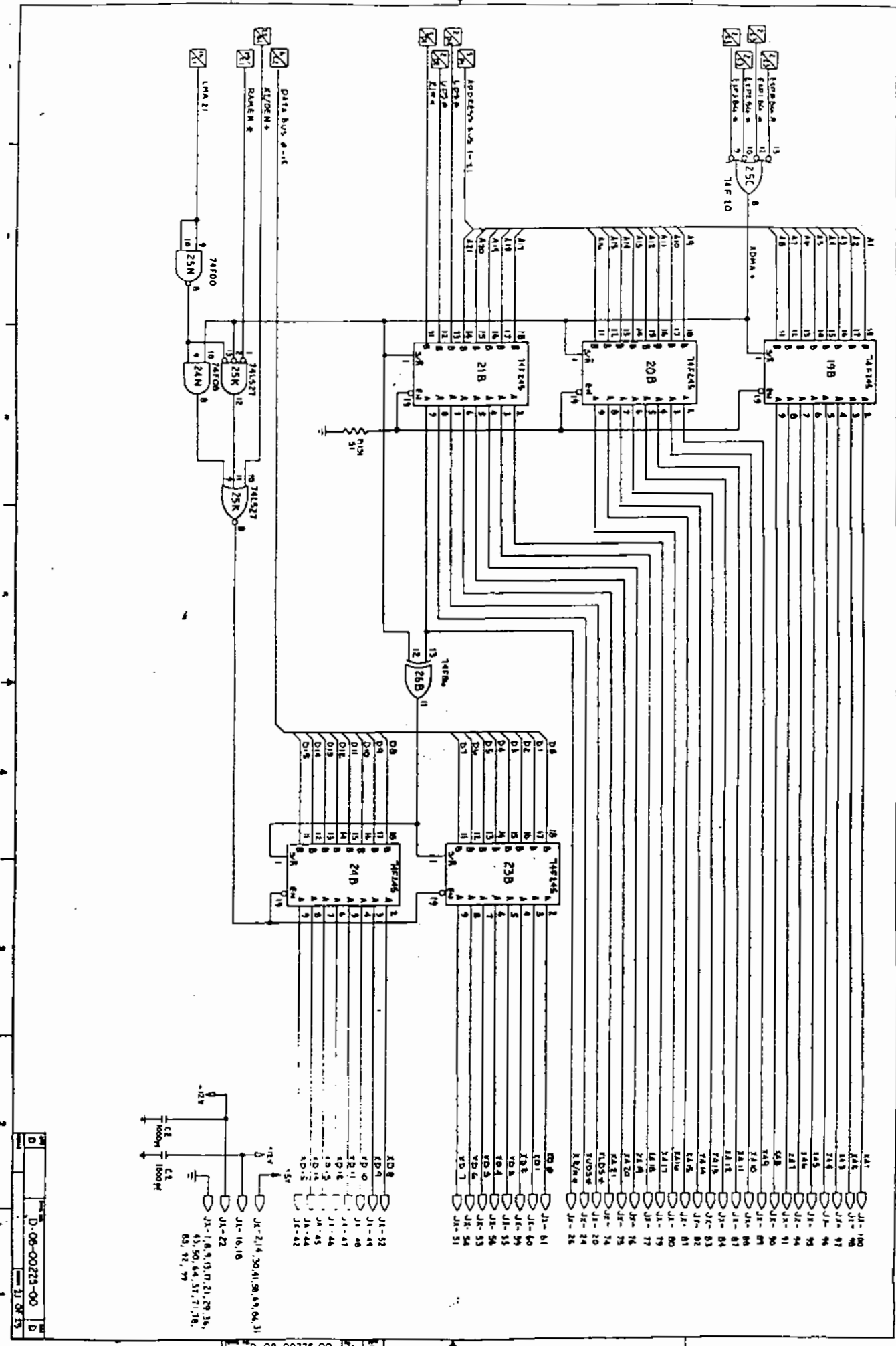






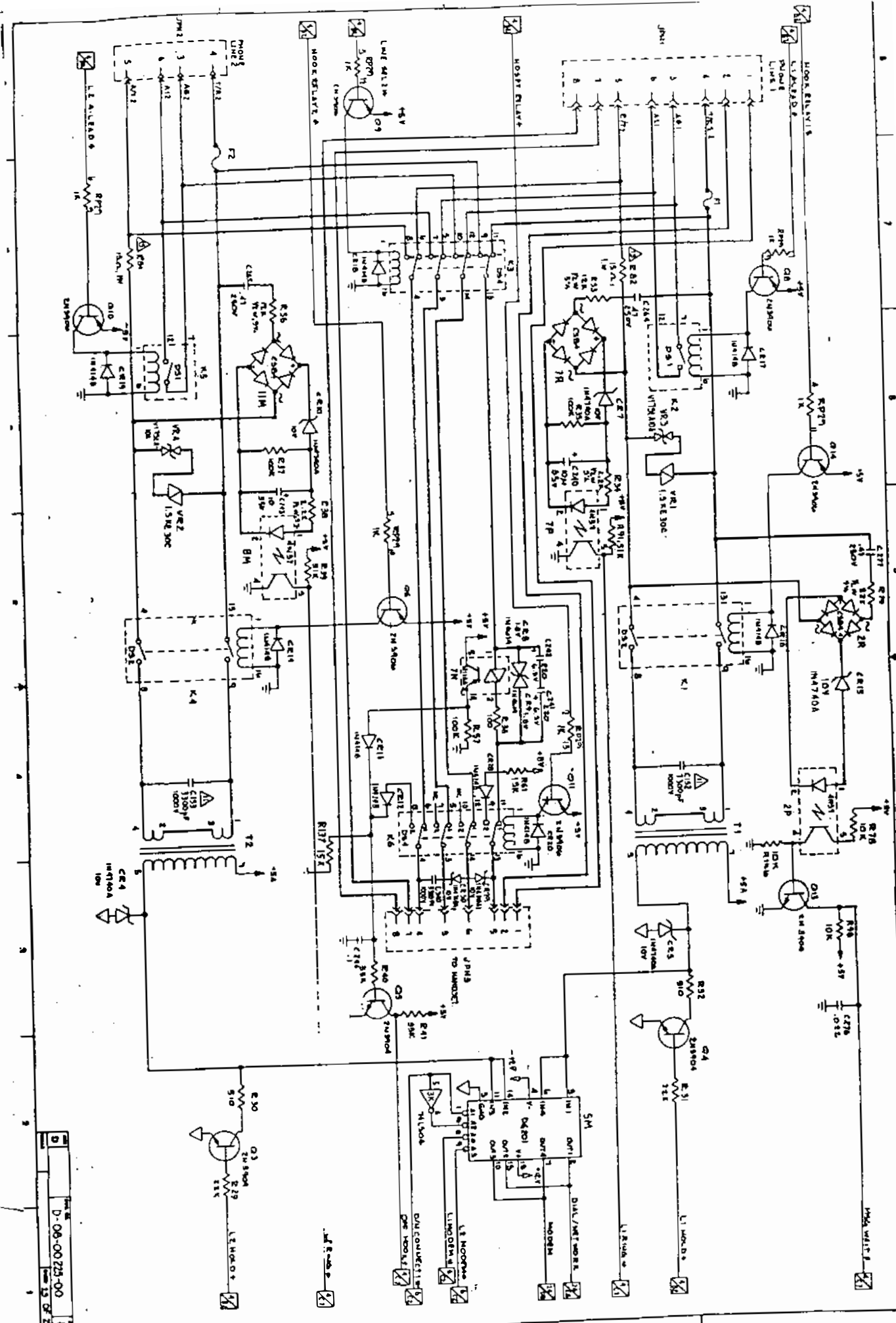
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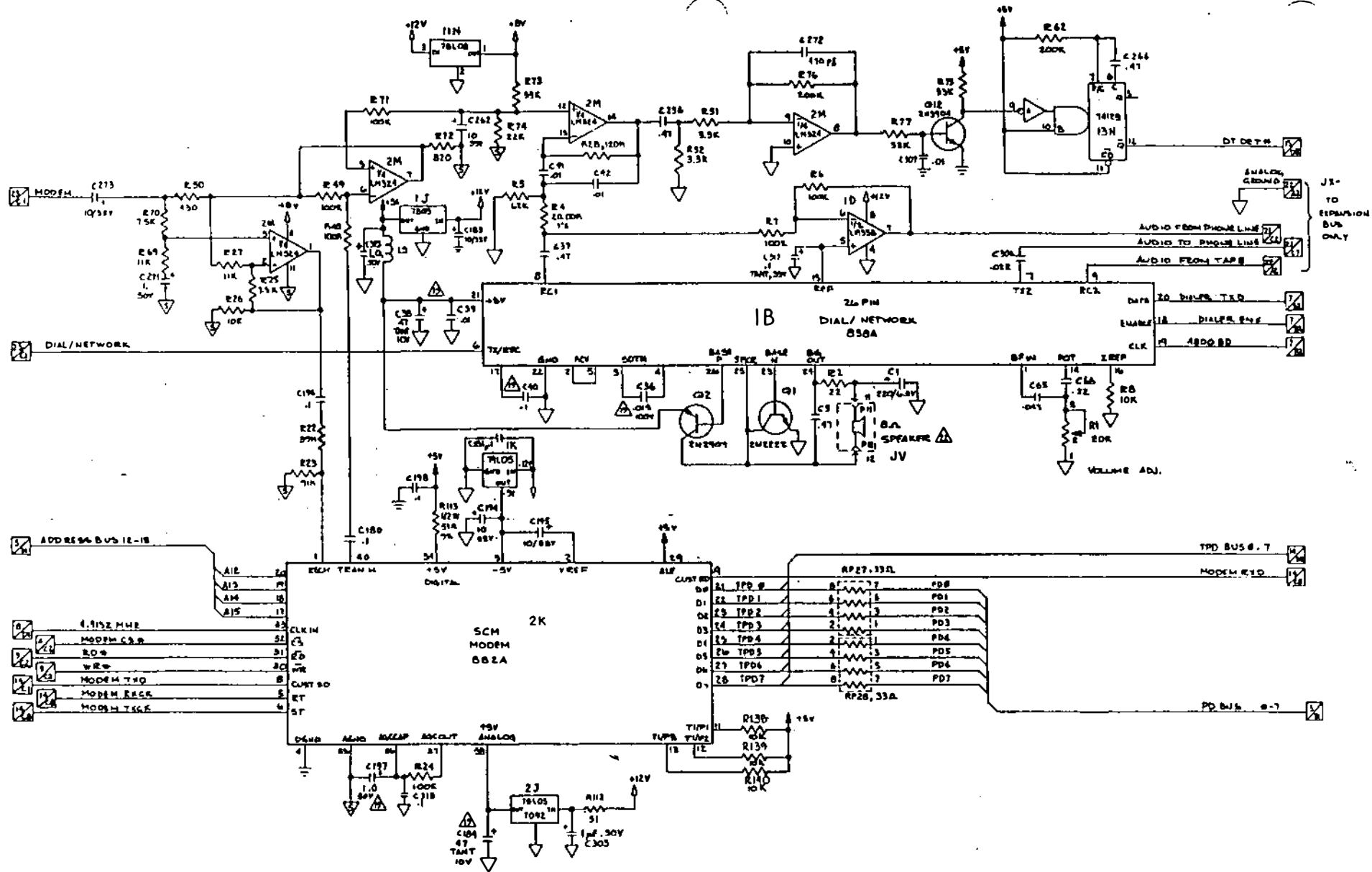
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I. C. VOLTAGE CHART				
DEVICE	REFERENCE DESIGNATION	PSW	DEND	PAGE NO.
74F00	22D, 23H	14	7	1, 4, 5, 14, 19, 21
74F02	16H, 27H	14	7	3, 4, 5, 14, 19, 22
74S03	15H	14	7	12
74LS04	3H	14	7	3, 5, 6, 17, 23
74F04	15H, 19F	14	7	2, 4, 12, 16
74F05	4J, 20E, 20F, 24H	14	7	1, 7, 14, 17, 21, 22
74LS06	12D, 12F	14	7	3, 4, 5, 14, 17, 19, 21
74LS08	13H	14	7	5, 17
74F10	13H	14	7	12
74F11	27F	14	7	2, 4
74LS14	4H, 10H	14	7	4, 5, 11, 13, 14
74F20	15C	14	7	1, 21
74LS27	23D, 23H, 24H	14	7	2, 4, 12, 16
74F31	3J, 13E, 14F, 24H, 24F, 24H	14	7	1, 3, 4, 5, 7, 9, 11, 14, 17, 19, 22
74S51	12H, 19H	14	7	5, 17
74F64	10G	14	7	3
74LS74	25H, 27H, 28H	16	8	2, 6, 7, 8, 11, 13
74F74	6H, 15H, 16H, 17H	14	7	4, 12, 17
74F06	24D	14	7	6, 21, 22
74S112	21E, 28G	16	8	3
74F23	13H	16	8	12, 24
74S124	14H	16	9	12
74LS130	24G, 27G, 28G	16	8	4
74F130	7J, 9J	16	8	17
74LS123	12F, 24H	16	8	5, 11, 13, 16
74F133	4J	16	8	17
74F153	14H	16	8	12
74LS157	19H, 19H	16	8	14
74F175	10D, 10H	16	8	3, 5
74LS248	17H, 24H	20	10	11, 13, 15
74LS244	9H, 15F, 16D, 14F, 23H, 24C	20	10	2, 4, 5, 6, 13, 15, 16, 17, 22
74F244	16F, 17F, 19G, 22B, 23G	20	10	2, 3, 5, 13, 15, 16, 22
74F245	11C, 12D, 13A, 13C, 13D, 17D, 19D, 20D, 21D, 23B, 23C, 24B, 24C	20	10	5, 8, 14, 19, 21
74F250	10J, 11F, 11G, 11H, 12E, 13D	16	8	17, 18
74LS259	7H, 18H	16	8	4, 6
74S168	27H	14	7	3
74LS273	17H, 27C	20	10	11, 13
74S279	14B, 15D	14	7	8
74LS340	10F	16	8	6
74LS373	14D, 14C, 21D, 24D, 25D	20	10	6
74F373	17G, 27F	20	10	5, 16
74F374	16H	20	10	2, 3, 4, 12
74LS374	16F, 27D	20	10	18
74LS393	16E, 20D	14	7	7
74F393	24F	14	7	4, 5, 8

I. C. VOLTAGE CHART				
DEVICE	REFERENCE DESIGNATION	PSW	DEND	PAGE NO.
74LS31	14H	16	8	6, 12, 14
74LS32	13H	16	8	12
74S00	13F 		7	14
74S01	10D, 28F	14	7	14
74S09	19C, 24C, 24C, 22C	18	9	16
74S12D	14C, 15C	28	14	5
74S18	15G	12	1	14
441G	14A, 15A, 16A, 17A	9	10	8
4756	1E, 3E, 4E, 5E, 6E, 7E, 8E, 9E, 10E, 11E, 12E, 13E, 14E, 15E, 16E, 17E, 18E, 19E, 20E, 21E, 22E, 23E, 24E, 25E, 26E, 27E, 28E, 29E, 30E, 31E, 32E, 33E, 34E, 35E, 36E, 37E, 38E, 39E, 40E, 41E, 42E, 43E, 44E, 45E, 46E, 47E, 48E, 49E, 50E, 51E, 52E, 53E, 54E, 55E, 56E, 57E, 58E, 59E, 60E, 61E, 62E, 63E, 64E, 65E, 66E, 67E, 68E, 69E, 70E, 71E, 72E, 73E, 74E, 75E, 76E, 77E, 78E, 79E, 80E, 81E, 82E, 83E, 84E, 85E, 86E, 87E, 88E, 89E, 90E, 91E, 92E, 93E, 94E, 95E, 96E, 97E, 98E, 99E, 100E	8	16	15, 20
68B18	14E	14, 19	6, 23	5
730A	1B			24
682A	2A			24
72B1	21H	40	20	14
CS04	24, 27, 11H			23
OG2H	3H			23
H11A2	7H			23
LM324	2H			24
LM325	1D			24
LF412	17H			12
4N37	2F, 7F, 8H			23
PAL16DA	24G	20	10	2
PAL16PA	14H	20	10	12
PAL16MA	24H	20	10	2
PAL16DA	25D	20	10	2
74S170P	24D	14, 19	6	15
WD100-05	21H	40	20	11
WD1157	12H	11	10	12
79L03	1H			24
7095	1J			24
70L05	11H			24
70L05	2J			24
YORD ARRAY	17C	40	20	7
ORA ORR ARRAY	22H	20	40	10
ORA ORR ARRAY	22E	20	40	7

Expansion Hardware

The expansion hardware provides additional memory and communication capabilities for the AT&T UNIX PC. The expansion hardware's EIA ports make it possible for the PC to communicate with another terminal or computer. Additional memory and EIA capabilities are available separately or in combination, as shown in the following list of expansion hardware options:

- o 0.5MB RAM Expansion Board (no EIA ports)
- o 2.0MB RAM Expansion Board (no EIA ports)
- o 0.5MB EIA/RAM Combo Board (two EIA ports)
- o 1.0MB EIA/RAM Combo Board (two EIA ports)
- o 1.5MB EIA/RAM Combo Board (two EIA ports)
- o Dual EIA Port Board (no RAM, two EIA ports)

The expansion hardware includes:

- o An interface connection P1 and associated circuitry
- o RAM memory
- o EIA connection circuitry (if an EIA or Combo board)

Interface Circuitry

All communications between the expansion board and the UNIX PC bus are through the expansion board interface connector P1.

Input/Output Handling

As a direct memory access (DMA) device data transfer from the expansion board to the PC bus causes the 68010 to wait while data is transferred into RAM memory. Data transfer is considered a fast cycle (500 ns).

Expansion Hardware

There are three functions which the expansion board may be called upon to perform. Read to memory, read from memory and port to or from memory to the RS-232 interface.

Expansion Board Schematic

Sheet 2--Memory Access Control Circuitry:

This circuitry consists of address latch 1K, lower and upper data strobe control, consisting of demultiplexers 3H and 3J and OR gates 3B and parity interrupt, 2C and 2E.

Sheet 3--Memory Bus Management and Communications Circuitry:

The upper portion of sheet 3 of the schematic contains map address management circuitry consisting of multiplexers 4A, 4B, 4C, 4E, 4H, and 4J. The lower portion of sheet 3 contains the communication interface IC 11E, RS-232 line drivers 12J, 12K, and 12A, and RS-232 receivers 11A and 12B and port connectors J1 and J2.

Note

This circuitry is only present on the EIA/RAM Combo and EIA/RAM boards. The 0.5 and 2.0 RAM expansion boards do not contain interface circuitry or RS-232 ports.

Sheets 4, 5 and 6--Memory (RAM) :

Memory circuitry consists of the X, Y, and Z bus, the read bus and read bus control 11H and 11C, and upper and lower parity generator IC,s 5K through 10K.

Depending on the amount of RAM that is mounted physically on the expansion board, these locations may or may not be used.

Sheet 5--Expansion Bus Interface:

The lower portion of sheet 5 of the schematic also contains data transceivers 1C and 1E connected to the read bus and expansion bus connector P1 completing the expansion loop.

IC DEVICE CHART				
IC TYPE	REFERENCE DESIGNATIONS	+5V	GND	UNUSED OUTPUTS
74F00	2A, 2H	14	7	
74F08	5A, 1H	14	7	
74F12	5B, 2J	14	7	
74F14	1D	14	7	
74F138	3E, 5H, 5J	16	8	
74F245	1C, 1E	20	18	
74F258	4A, 4D, 4C, 4E, 4H, 4J, 5B, 5H	18	8	
74F373	1H	20	18	
74F85	1J	16	8	
74LS125	1A, 11D	14	7	
74LS125	11H	16	8	
74LS280	2C, 2E	14	7	
1488	12A, 12J	14	7	
1489	11A, 12D, 12H	14	7	
8530	11E	2	24	
48256	5A, 5D, 5C, 5E, 5F, 5H, 5J, 5K, 6A, 6D, 6C, 6E, 6F, 6H, 6J, 6K, 7A, 7D, 7C, 7E, 7F, 7H, 7J, 7K, 8A, 8D, 8C, 8E, 8F, 8H, 8J, 8K, 9A, 9D, 9C, 9E, 9F, 9H, 9J, 9K, 10A, 10D, 10C, 10E, 10F, 10H, 10J, 10K	8	16	
74F06	2D	14	7	
74125	2H, 11H	16	8	
74LS574	11C	20	18	
DL	3C	14	7	

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	USED BUT NOT SHOWN
C125	C4, C5, C19	C18
J2		
P1		
P10		
P12		
P2		
W5		

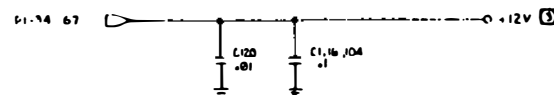
SPARES (EXC 2C5)	
PART	UNUSED PINS
RP6	1, 2
RV1	1, 2
RP3	1, 2
RP11	3, 4, 5, 6
J1	1, 9, 10, 11, 12, 13, 14, 16, 18, 19, 21, 22, 23
J2	1, 9, 10, 11, 12, 13, 14, 16, 18, 19, 21, 22, 23
P1	16, 17, 40, 42, 43, 44, 45, 54, 55, 57, 60, 61, 62, 63, 69, 71, 73

PARTS AFFECTED BY VERSION												
AWAY FROM BOARD	VERSION	CHANGING PART	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10
-01	QUINTE											
-01	QUINTE											
-02	QUINTE											
-03	1.5 MBYTE											

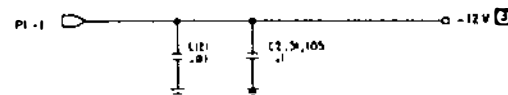
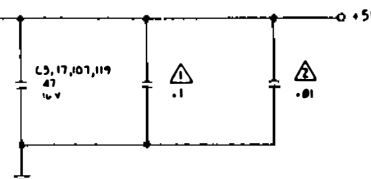
INCHES		MILLIMETERS		PARTS LIST	
				Convergent Technologies	
THIS DRAWING IS THE PROPERTY OF CONVERGENT TECHNOLOGIES. IT IS TO BE USED FOR THE PURPOSES SPECIFIED IN THE ORDER. IT IS NOT TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF CONVERGENT TECHNOLOGIES.		DATE: 10/11/91 BY: [Signature] CHECKED: [Signature]		SCHEMATIC, 34 COMBO CARD D-06-00221-00 1 OF 6	

REV	DESCRIPTION	DATE	BY	CHKD
A	RELEASE TO CONTROL			
B	REVISED PER C.D. 8 5190			
C	REVISED PER C.D. 8 9203			
D	REVISED PER C.D. 8 9201			
DA	PER RECORD CHANGE 8 D-028			

P1-4, 5, 7, 8, 18, 11, 15, 16, 19, 21, 22, 24, 25, 27, 32, 33



P1-3, 4, 9, 12, 15, 20, 23, 26



4, 6, 8, 11, 15, 16, 21, 22, 13, 25, 27, 29, 30, 4, 45, 46, 47, 48, 51, 53, 55, 57, 60, 61, 62, 64, 66, 68, 69, 71, 73, 75, 77, 80, 82, 84, 94, 95, 97, 98, 100, 102, 113, 114, 116, 118

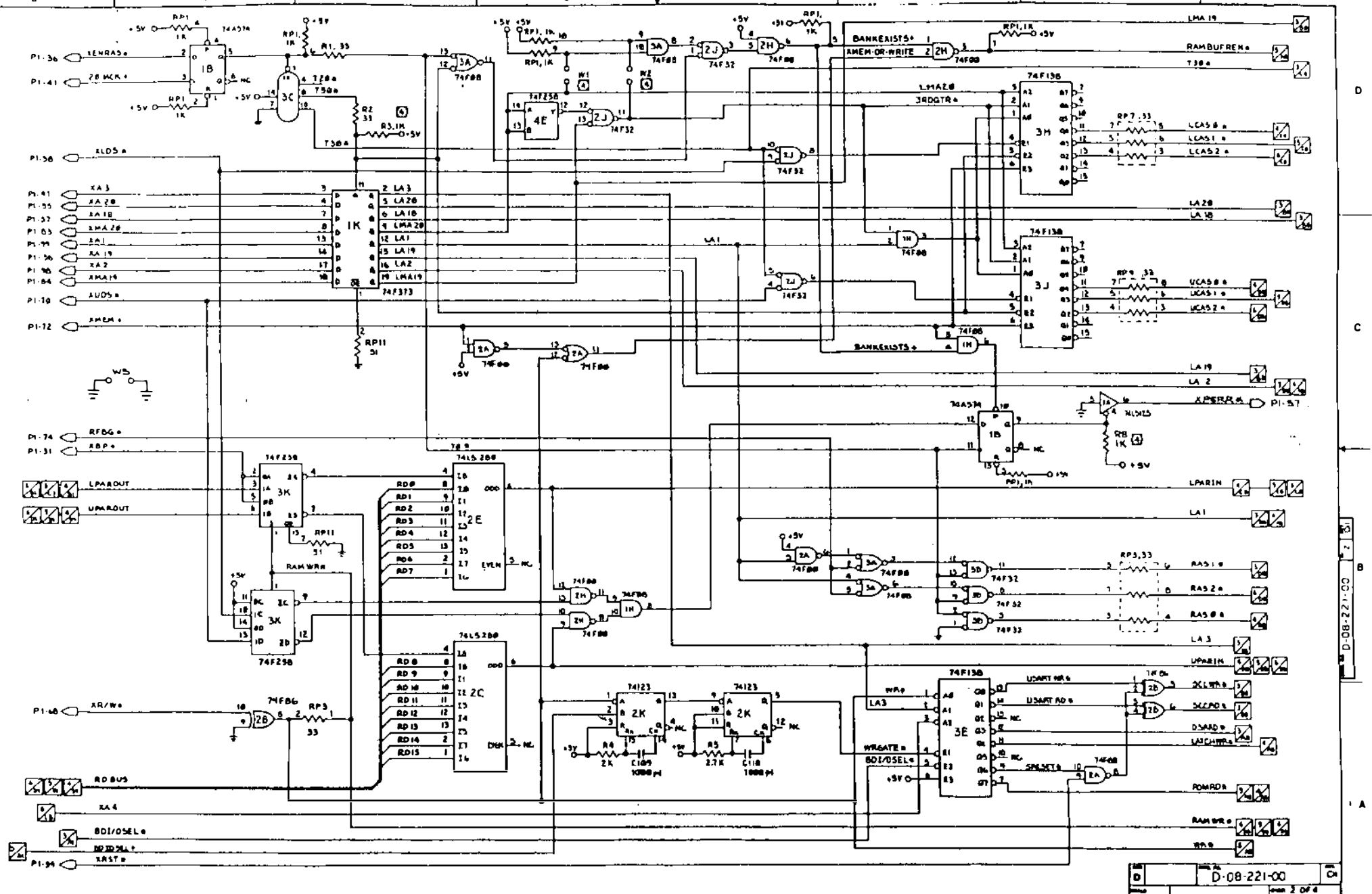
15, 16, 12, 14, 15, 24, 26, 28, 42, 44, 46, 49, 50, 52, 54, 56, 58, 63, 65, 67, 18, 12, 14, 16, 18, 81, 83, 85, 86, 88, 104, 106, 110, 112, 113, 115, 117

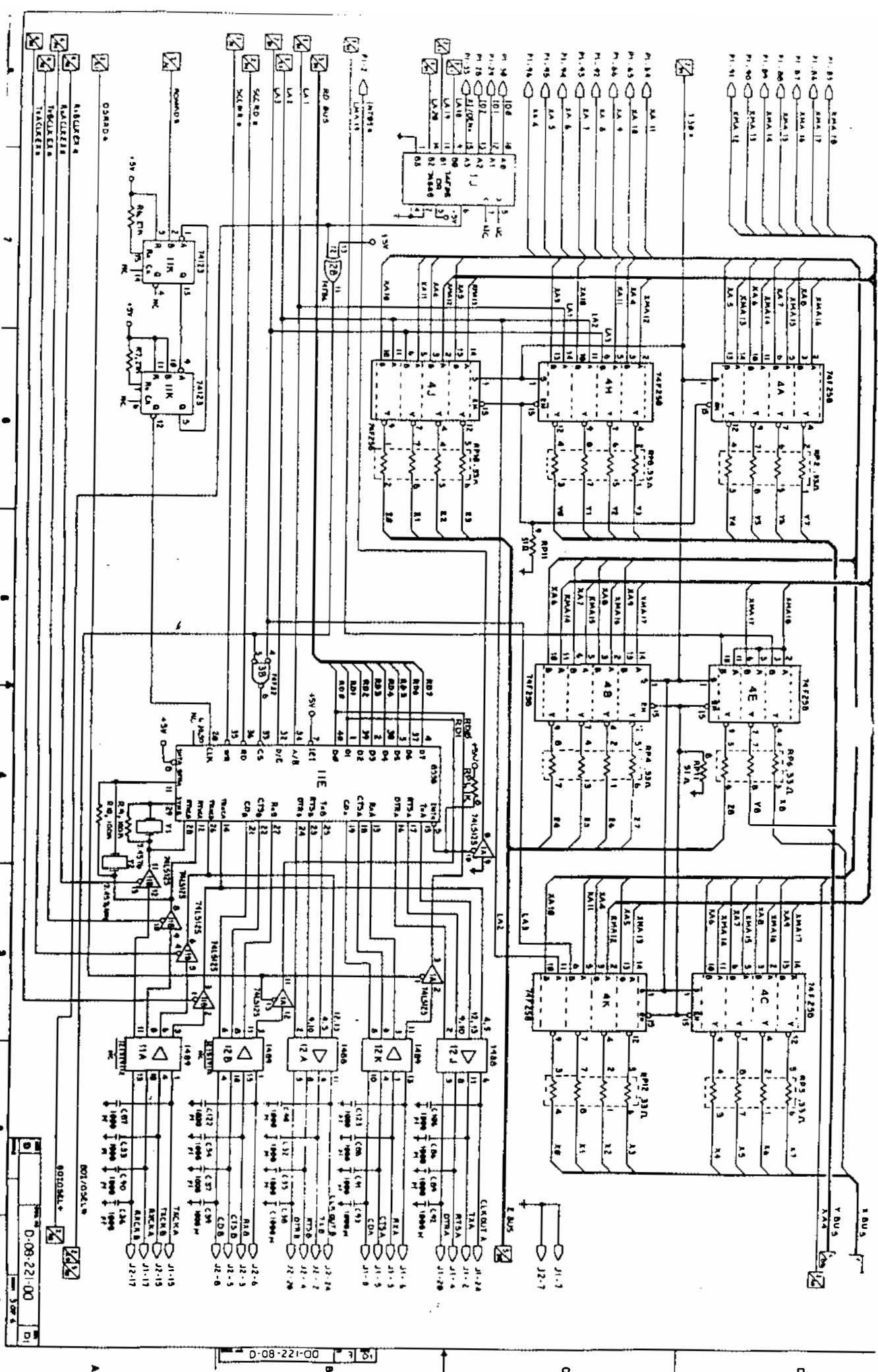
DIVISION I.D.
IDENTIFIES AS PER
BASIC PART NUMBER
VERSION NUMBER
D-60-00221-XX REV X

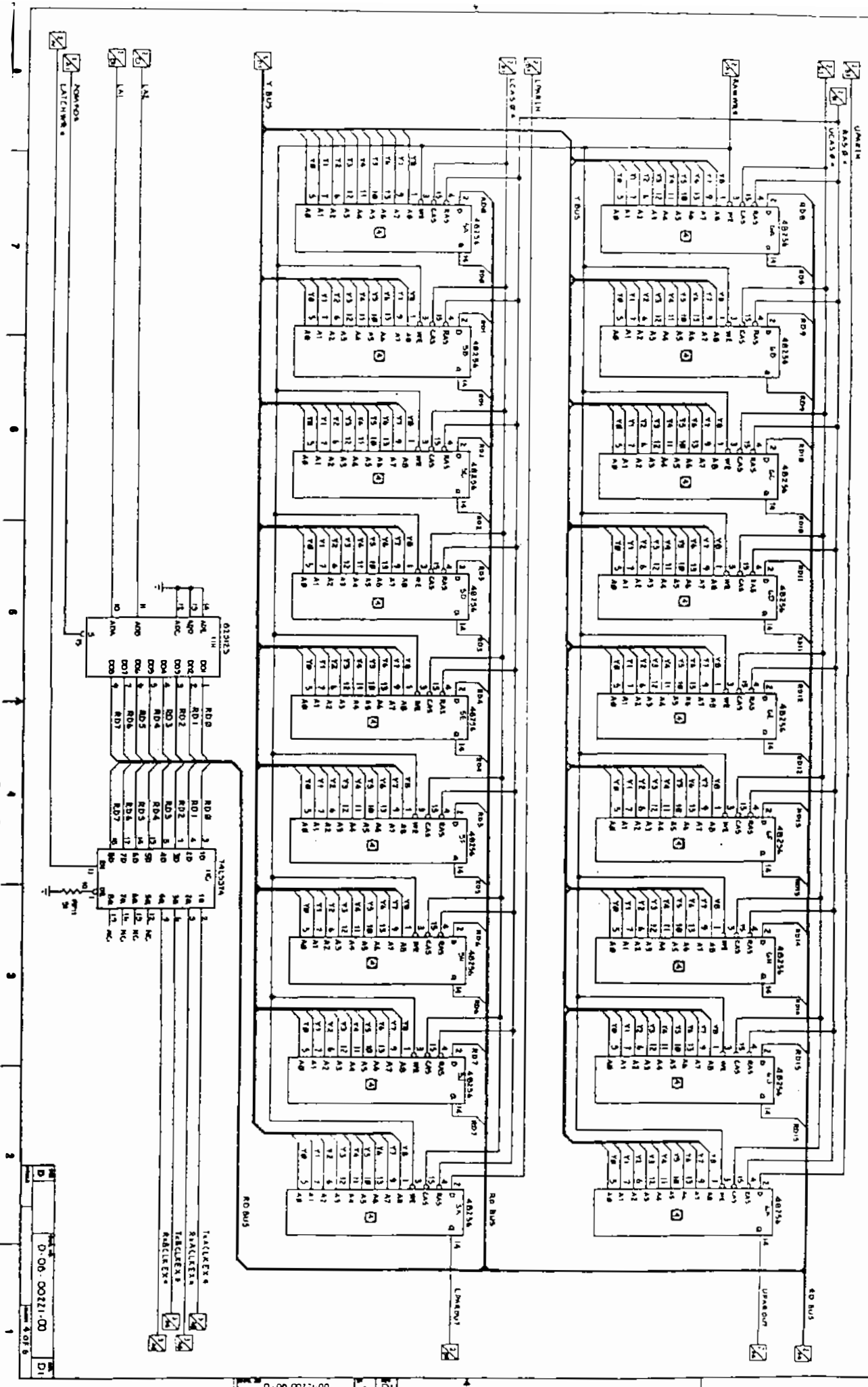
NOTES: UNLESS OTHERWISE SPECIFIED

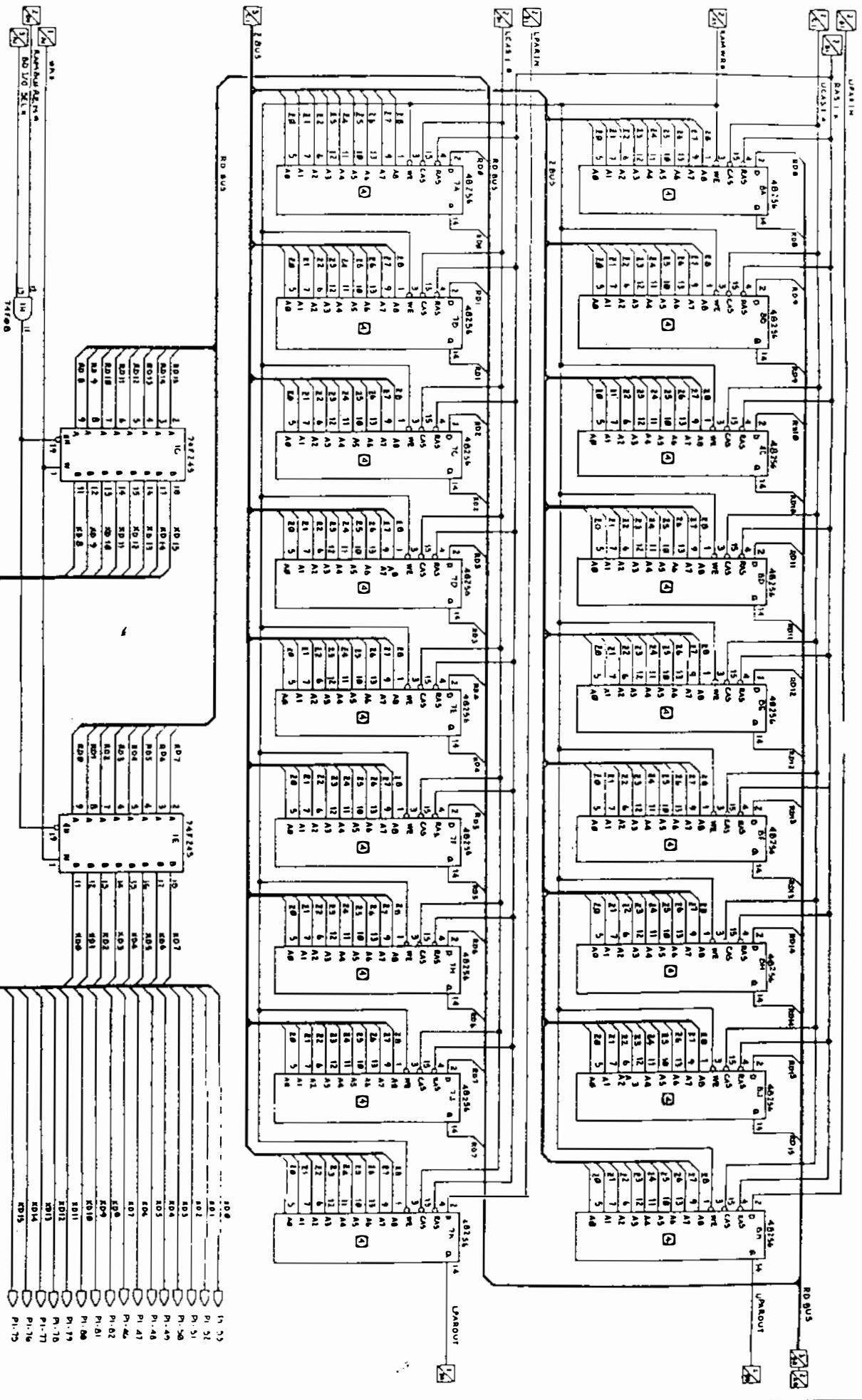
- ALL RESISTOR VALUES ARE IN OHMS, 100K, 5%.
- ALL CAPACITOR VALUES ARE IN MICROFARADS.
- CONNECT PIN 14 OF ALL 7400S TO +12V.
- CONNECT PIN 1 OF ALL 7400S TO -12V.
- PART AFFECTED BY VERSION; SEE TABLE.

PAGE NUMBER SHOWN AS:
34-21 NO
ZONE







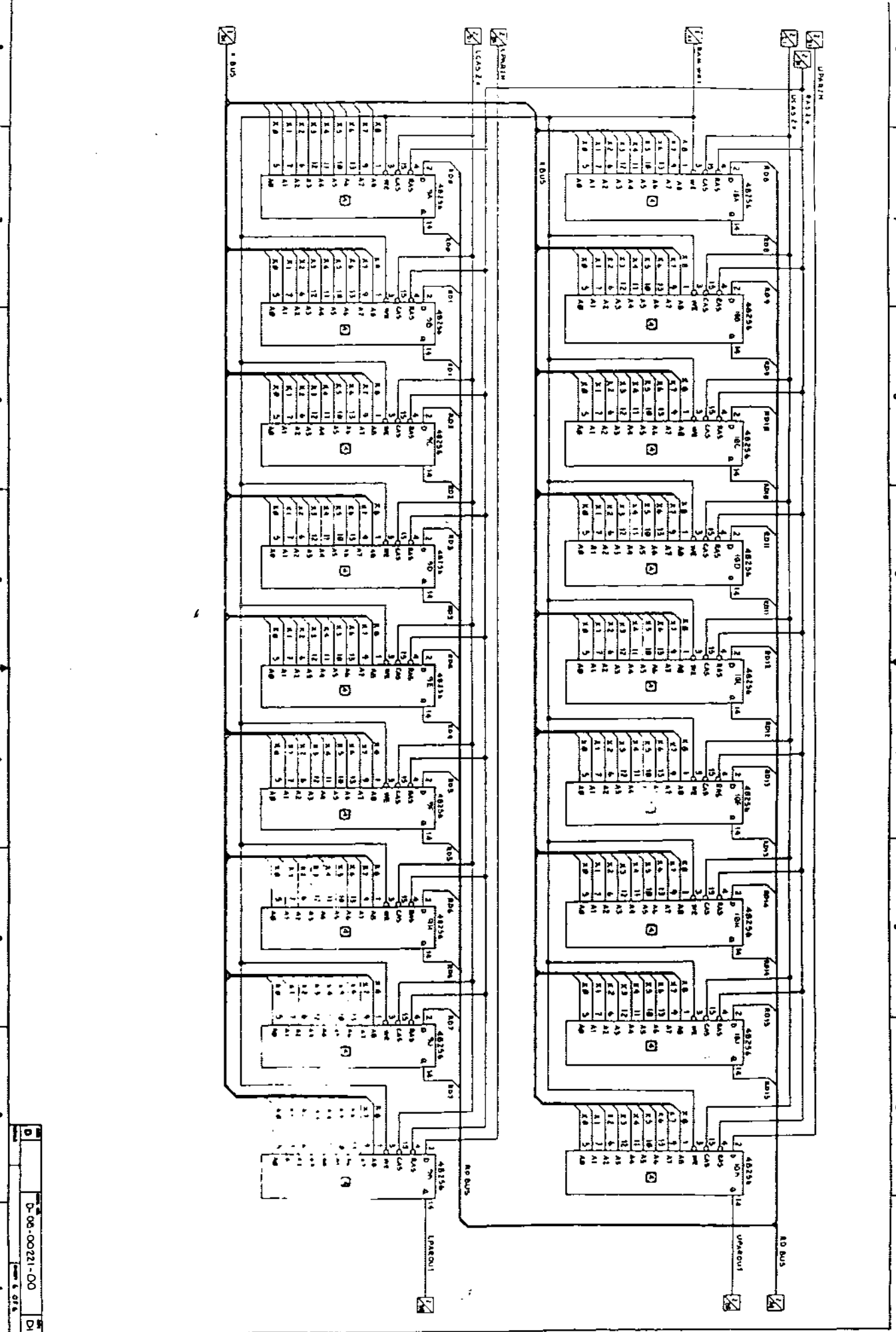


0-06.00221-00

1

5000

DI

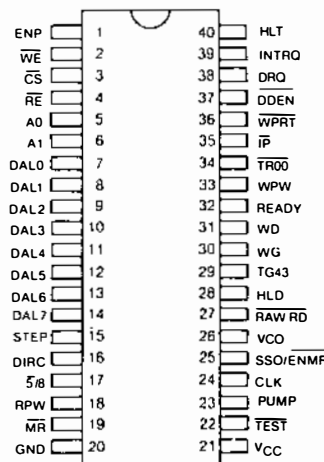


WD279X-02 Floppy Disk Formatter/Controller Family

WD279X-02

FEATURES

- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
 - IBM 3740 (FM)
 - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTIPLE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
 - SELECTABLE TRACK-TO-TRACK ACCESS
 - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY



PIN DESIGNATION

DESCRIPTION

The WD279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The WD279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The WD279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and WD279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical.

Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The WD279X is set up to operate on a multiplexed bus with other bus-oriented devices.

The WD279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The 2793 is identical to the 2791 except the DAL lines are TRUE for systems that utilize true data busses.

The 2795/7 has a side select output for controlling double sided drives.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION																									
1	ENABLE PRECOMP	ENP	A Logic high on this input enables write precompensation to be performed on double density Write Data output only.																									
19	MASTER RESET	MR	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.																									
20	POWER SUPPLIES	VSS	Ground																									
21		VCC	+5V $\pm$ 5%																									
COMPUTER INTERFACE:																												
2	WRITE ENABLE	WE	A logic low on this input gates data on the DAL into the selected register when CS is low.																									
3	CHIP SELECT	CS	A logic low on this input selects the chip and enables computer communication with the device.																									
4	READ ENABLE	RE	A logic low on this input controls the placement of data from a selected register on the DAL when CS is low.																									
5, 6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under RE and WE control: <table><tr><td>CS</td><td>A1</td><td>A0</td><td>RE</td><td>WE</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Status Reg</td><td>Command Reg</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Track Reg</td><td>Track Reg</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Sector Reg</td><td>Sector Reg</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Data Reg</td><td>Data Reg</td></tr></table>	CS	A1	A0	RE	WE	0	0	0	Status Reg	Command Reg	0	0	1	Track Reg	Track Reg	0	1	0	Sector Reg	Sector Reg	0	1	1	Data Reg	Data Reg
CS	A1	A0	RE	WE																								
0	0	0	Status Reg	Command Reg																								
0	0	1	Track Reg	Track Reg																								
0	1	0	Sector Reg	Sector Reg																								
0	1	1	Data Reg	Data Reg																								
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on WD2791 and WD2795.																									
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz $\pm$ 1% for 8" drives, 1 MHz $\pm$ 1% for mini-floppies.																									
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.																									
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command and is reset when the Status register is read or the Command register is written to.																									
FLOPPY DISK INTERFACE:																												
15	STEP	STEP	The step output contains a pulse for each step.																									
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.																									
17	5¼," 8" SELECT	5/8	This input selects the internal VCO frequency for use with 5¼" drives or 8" drives.																									
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.																									
22	TEST	TEST	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.																									

PIN DESCRIPTION (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
23	PUMP	PUMP	High-Impedance output signal which is forced high or low to increase/decrease the VCO frequency.
25	ENABLE MINI-FLOPPY (2791, 2793)	ENMF	A logic low on this input enables an internal $\div 2$ of the Master Clock. This allows both 5 1/4" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1.
25	SIDE SELECT OUTPUT (2795, 2797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO center frequency.
27	RAW READ	RAW READ	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	MFM or FM output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	TRACK 00	TA00	This input informs the WD279X that the Read/Write head is positioned over Track 00.
35	INDEX PULSE	IP	This input informs the WD279X when the index hole is encountered on the diskette.
36	WRITE PROTECT	WPRT	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	DDEN	This input pin selects either single or double density operation. When $\overline{\text{DDEN}} = 0$, double density is selected. When $\overline{\text{DDEN}} = 1$, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

WD279X-02

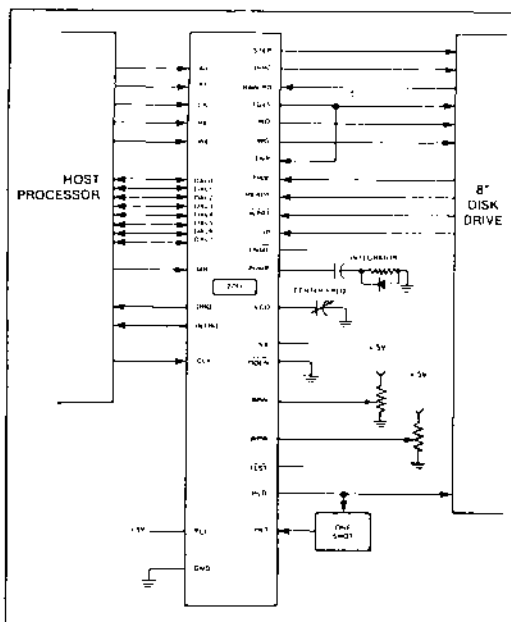


Figure 1.

APPLICATIONS

8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER

The WD279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation may be enabled, its value predetermined by an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

The WD279X is fabricated in NMOS silicon gate technology and available in a 40 pin dual-in-line package.

FEATURES	2791	2793	2795	2797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Side Select Out			X	X
Internal CLK Divide	X	X		

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations in Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrements and is used for register modification and comparisons with the disk recorded ID field.

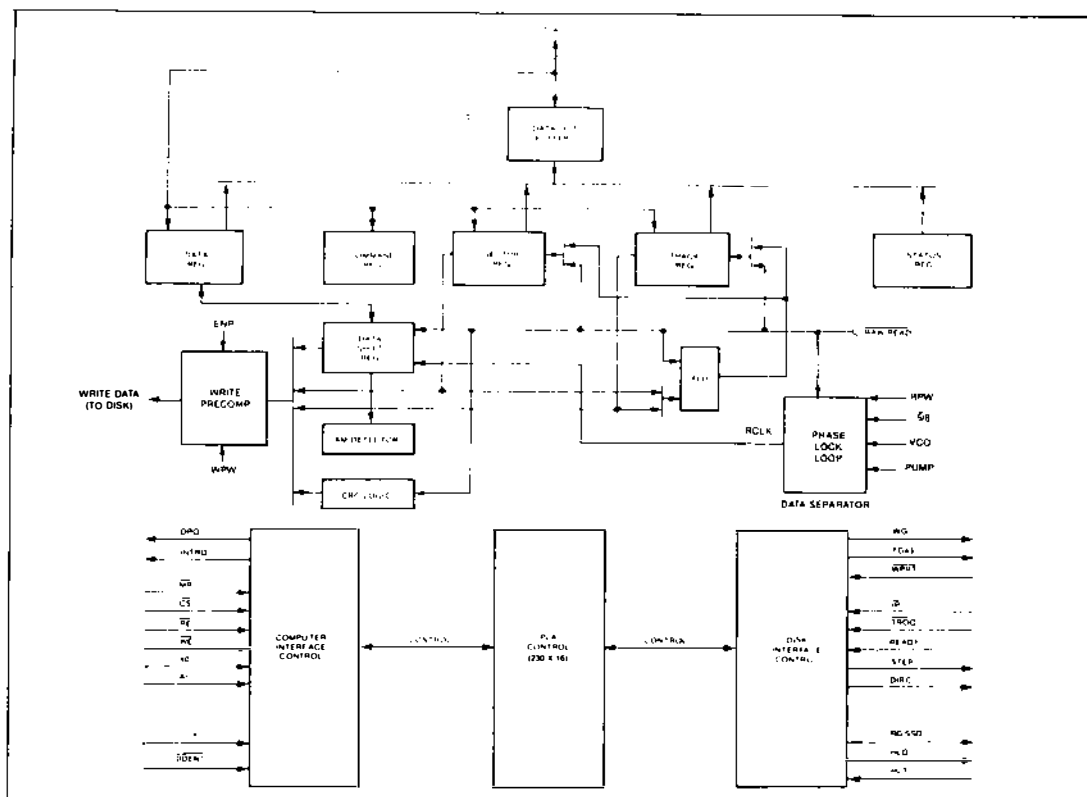
Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation — enables write precompensation to be performed on the Write Data output.

etects ID, data
e operations.
compensation

REPORT



WD279X BLOCK DIAGRAM

Data Separator — a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD279X. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\bar{R}\bar{E}$)	WRITE ($\bar{W}\bar{E}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the $\$$ Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 279X has two modes of operation according to the state of DDEN (Pin 37). When DDEN = 1, Single Density (FM) is selected. When DDEN = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5¼" drives.

On the 2791/2793, the ENMF input (Pin 25) can be used for controlling both 5¼" and 8" drives with a single 2 MHz clock. When ENMF = 0, an internal $\div 2$ of the CLK is performed. When ENMF = 1, no divide takes place. This allows the use of a 2 MHz clock for both 5¼" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The 5/8 input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When 5/8 = 0, 5¼" data separation is selected; when 5/8 = 1, 8" drive data separation is selected.

CLOCK (24)	ENMF (25)	5/8 (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

FUNCTIONAL DESCRIPTION

The WD279X-02 is software compatible with the FD179X-02 series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the 179X, the 279X contains an internal Data Separator and Write precompensation circuit. The TEST (Pin 22) line is used to adjust both data separator and precompensation. When TEST = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with TEST = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The TEST line also contains a pull-up resistor, so adjustments can be performed simply by grounding the TEST pin, overriding the pull-up. The TEST pin cannot be used to disable stepping rates during operation as its function is quite different from the 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, 5/8, ENMF, WPRT, DDEN, HLT, TEST, and MR.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1." For MFM formats, DDEN should be

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

* 2795/97 may vary — see command summary.

placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

The WD279X recognizes tracks and sectors numbered 00-FFX. However, due to programming restrictions, only tracks and sectors 00 thru F4 can be formatted.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 279X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the 279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

A. Command

Type	Command
I	Resto
I	Seek
I	Step
I	Step-i
I	Step-c
II	Read
II	Write
III	Read
III	Read
III	Write
IV	Force

FLAG SUMMARY

Command Type	Flag
I	
I	
I	
I	
II & II	
II	
II & II	
II & II	
II	
II	
IV	

*NOTE: See

TABLE 1. COMMAND SUMMARY

A. Commands for Models: 2791, 2793

B. Commands for Models: 2795, 2797

Type	Command	Bits								Bits							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r1	r0	0	0	0	0	h	V	r1	r0
I	Seek	0	0	0	1	h	V	r1	r0	0	0	0	1	h	V	r1	r0
I	Step	0	0	1	T	h	V	r1	r0	0	0	1	T	h	V	r1	r0
I	Step-in	0	1	0	T	h	V	r1	r0	0	1	0	T	h	V	r1	r0
I	Step-out	0	1	1	T	h	V	r1	r0	0	1	1	T	h	V	r1	r0
II	Read Sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	S	E	C	a0	1	0	1	m	L	E	U	a0
III	Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	l3	l2	l1	l0	1	1	0	1	l3	l2	l1	l0

TABLE 2. FLAG SUMMARY

FLAG SUMMARY

TABLE 2 FLAG SUMMARY

Command Type	Bit No(s)		Description																				
I	0, 1	r1 r0 = Stepping Motor Rate See Table 3 for Rate Summary																					
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track																				
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning																				
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register																				
II & III	0	a0 = Data Address Mark	a0 = 0, FB (DAM) a0 = 1, F8 (deleted DAM)																				
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare																				
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1																				
II & III	2	E = 15 MS Delay	E = 0, No. 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)																				
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1																				
II	3	L = Sector Length Flag	<table><tr><th colspan="5">LSB's Sector Length in ID Field</th></tr><tr><th></th><th>00</th><th>01</th><th>10</th><th>11</th></tr><tr><td>L = 0</td><td>256</td><td>512</td><td>1024</td><td>128</td></tr><tr><td>L = 1</td><td>128</td><td>256</td><td>512</td><td>1024</td></tr></table>	LSB's Sector Length in ID Field						00	01	10	11	L = 0	256	512	1024	128	L = 1	128	256	512	1024
LSB's Sector Length in ID Field																							
	00	01	10	11																			
L = 0	256	512	1024	128																			
L = 1	128	256	512	1024																			
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records																				
IV	0-3	l _x = Interrupt Condition Flags l ₀ = 1 Not Ready To Ready Transition l ₁ = 1 Ready To Not Ready Transition l ₂ = 1 Index Pulse l ₃ = 1 Immediate Interrupt, Requires A Reset* l ₃ -l ₀ = 0 Terminate With No Interrupt (INTRQ)																					

*NOTE: See Type IV Command Description for further information.

Write Precompensation

When operating in Double Density mode ($\overline{DDEN} = 0$), the 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST} = 0$.

Data Separation

The 279X can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST} = 0$. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a Logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of 5-60 pf is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

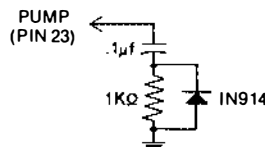
The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance

must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5 1/4" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22µf.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field ($r_0 r_1$), which determines the stepping motor rate as defined in Table 3.

A 2µs (MFM) or 4µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK	R1	R0	2 MHz	1 MHz
			$\overline{TEST} = 1$	$\overline{TEST} = 1$
0	0	0	3 ms	6 ms
0	0	1	6 ms	12 ms
1	1	0	10 fns	20 ms
1	1	1	15 ms	30 ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 ($V = 1$) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID

Field is con
Register. If th
Cyclic Redu
operation is c
errors. If there
status bit is s
field is read fr

The WD279X
number and c
otherwise the
If $V = 0$, no v

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upon receipt
active it rem
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Head Load ti
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The low to hi
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and supplied

When both t
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pears as stat

In summary
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and the 279X
HLD is set al
of the comm
internal 15 m
to occur.

For Type II a
active and HI
made active,
sampled unti

RESTORE (S)

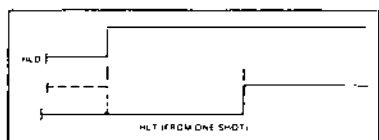
Upon receipt
sampled. If
head is posit
with zeroes

Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The WD279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the 279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the 279X which is used for the head engage time. When HLT = 1, the 279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLT is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 279X.



HEAD LOAD TIMING

When both HLD and HLT are true, the 279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the 279X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the 279X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

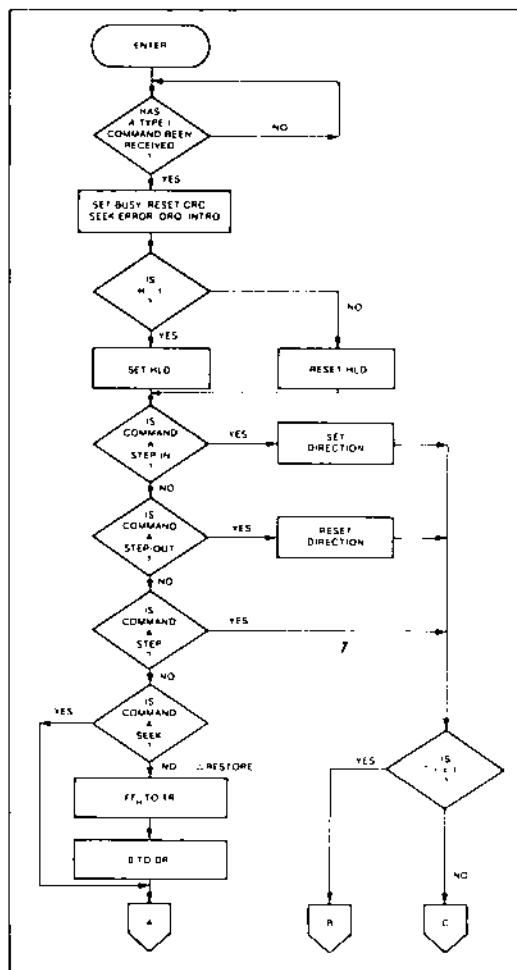
RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 (TR00) input is sampled. If TR00 is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If TR00 is not

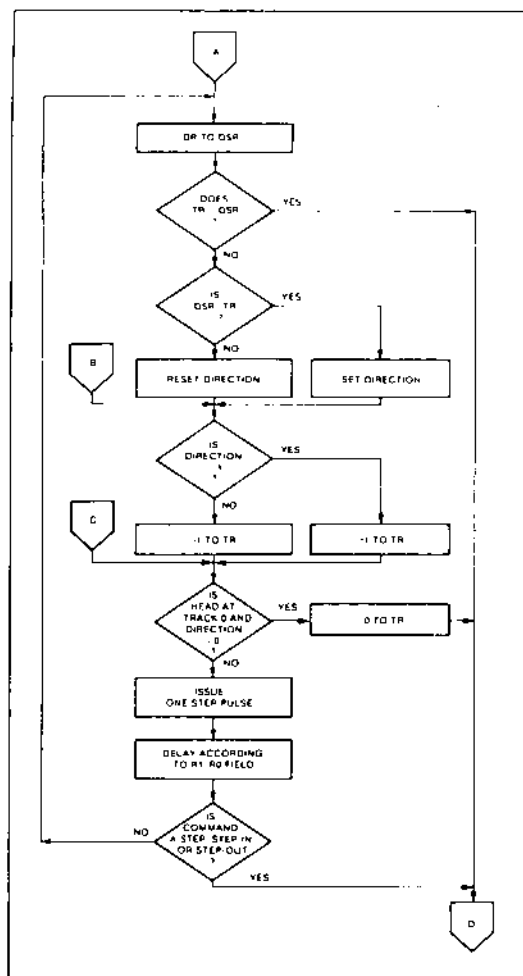
active low, stepping pulses at a rate specified by the r1r0 field are issued until the TR00 input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the 279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

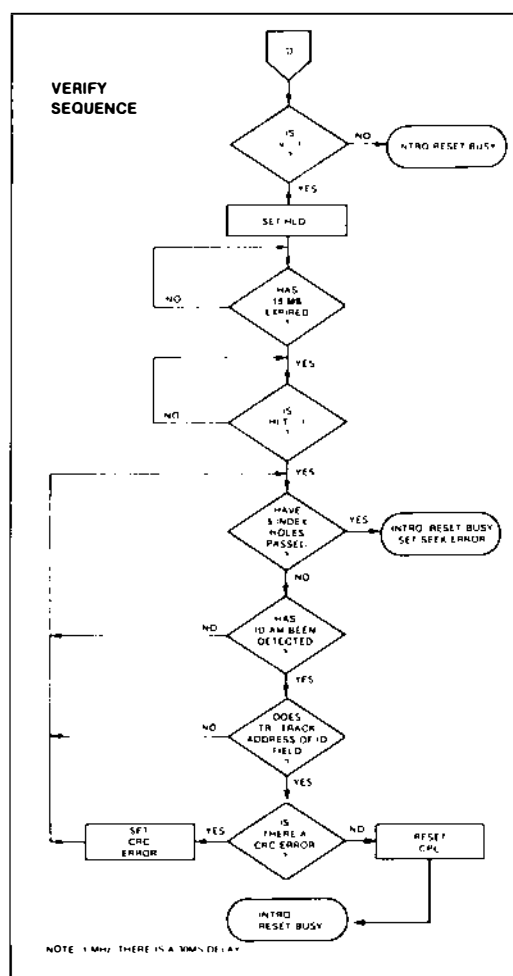
contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the 279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the $r1f0$ field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a

VERIFY SEQUENCE

TYPE I COMMAND FLOW

delay determined by the $r1f0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the $r1f0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

TYPE II COMMANDS

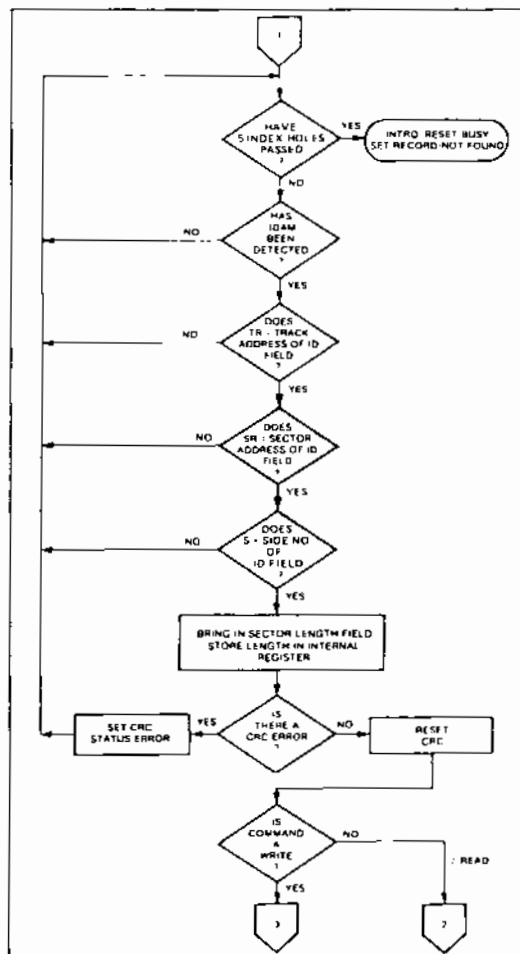
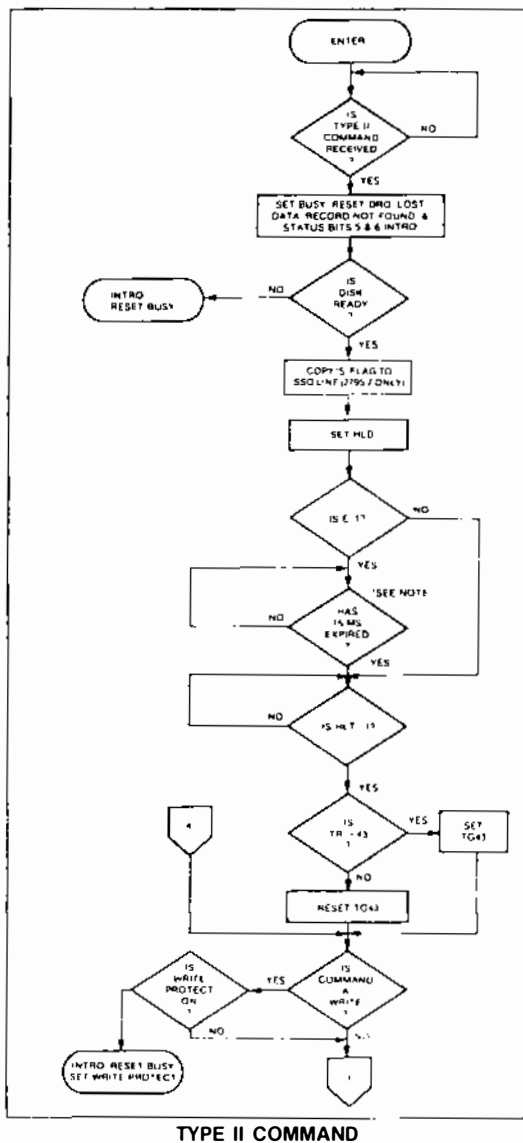
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the

Sector Register receipt of the the E flag = 1 and HLT is set the head is located

When an ID for the Track Number there is not a and a compare Sector Number Register. If the countered ID again made. I then located

Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

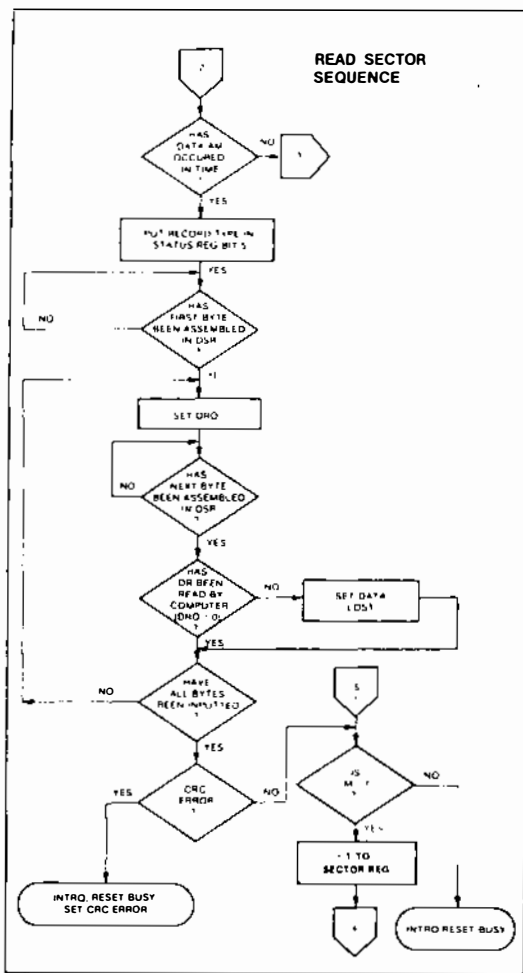
When an ID field is located on the disk, the 279X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from



depending upon the command. The 279X must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 4) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If $m = 0$, a single sector is read or written and an interrupt is generated at the completion of the command. If $m = 1$, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 279X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the 279X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds

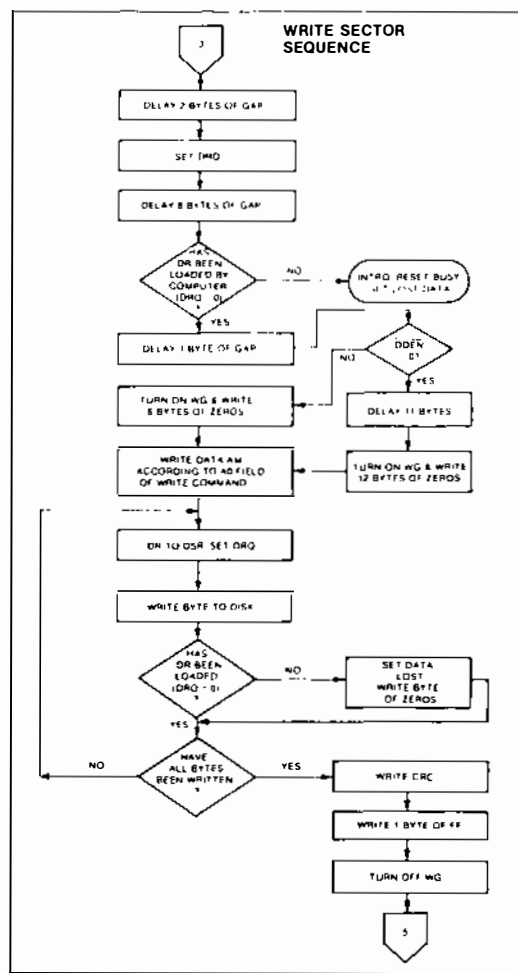
**TYPE II COMMAND**

the number available. The 279X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 2791-93 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the 279X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 2795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 2795/7 READ SECTOR and WRITE SECTOR com-

**TYPE II COMMAND**

mands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred

that character is loaded. This sequence can be input to the end of the data field command is term command).

At the end of the R Mark encountered Register (Bit 5) as s

STATUS
BIT 5

1	C
0	C

WRITE SECTOR

Upon receipt of t loaded (HLD active ID field is encount correct sector nu CRC, a DRQ is ge single density and field and the Write DRQ is serviced computer). If DRC terminated and th has been service zeroes in single d then written on Mark is then writ field of the comm

ag

1
0

The 279X then wr the computer. If tinuous writing th zeroes is written minated. After th disk, the two-byt on the disk follow WG output is th INTRQ will set i written. For parti write the data an chip fill the zero status and impro

TYPES III COMM READ ADDRESS

Upon receipt of loaded and the countered ID fie data bytes of the the DR, and a DF of the ID field are

TRACK ADDR	S NUI
1	

Although the

that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 279X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $\alpha 0$ field of the command as shown below:

$\alpha 0$	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The 279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μ sec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

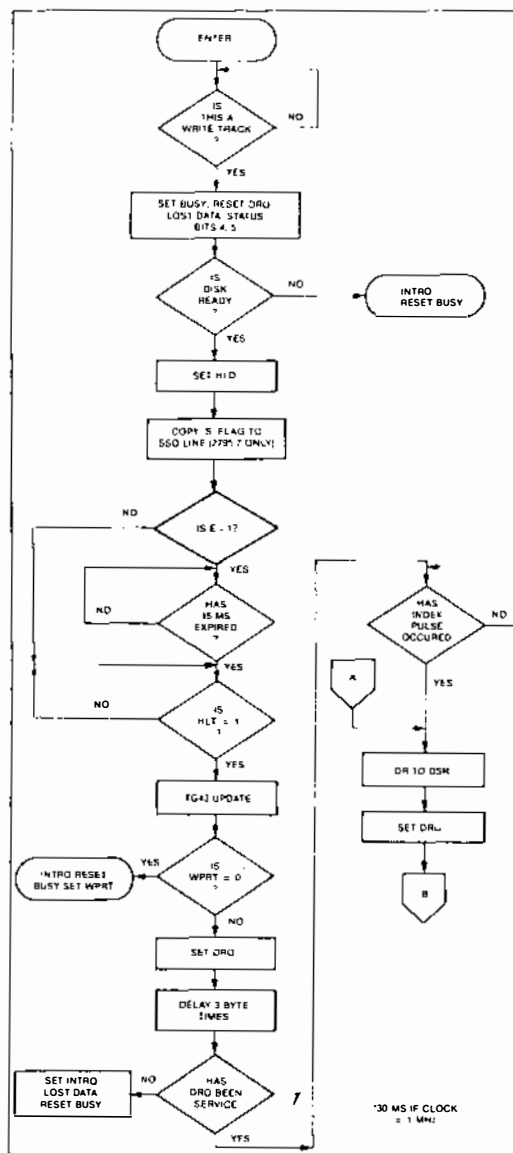
TYPES III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the

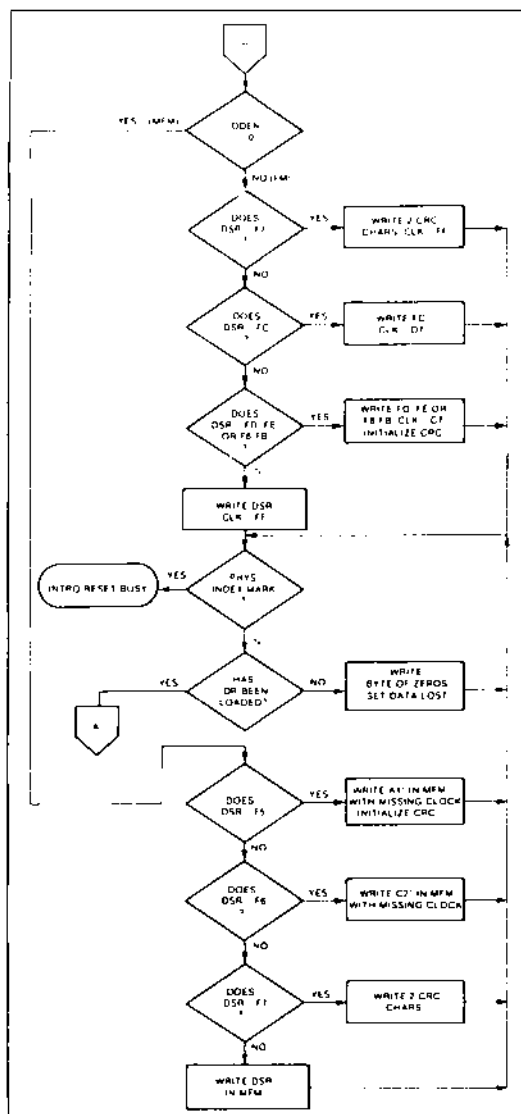


TYPE III COMMAND WRITE TRACK

computer, the 279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The ac-



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	WD279X INTERPRETATION IN FM (DDEN = 1)	WD279X INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

* Missing clock transition between bits 4 and 5

** Missing clock transition between bits 3 and 4

accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule with the Lost Data status flag being set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 279X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR

or by receipt of F5 in CRC characters in F patterns F5 thru FE fields, or ID fields. Also pattern.

Disks may be formatted with sector lengths of

TYPE IV COMMANDS

The Forced Interrupt terminate a multiple sector Type I status in the command will be loaded into the command will be

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

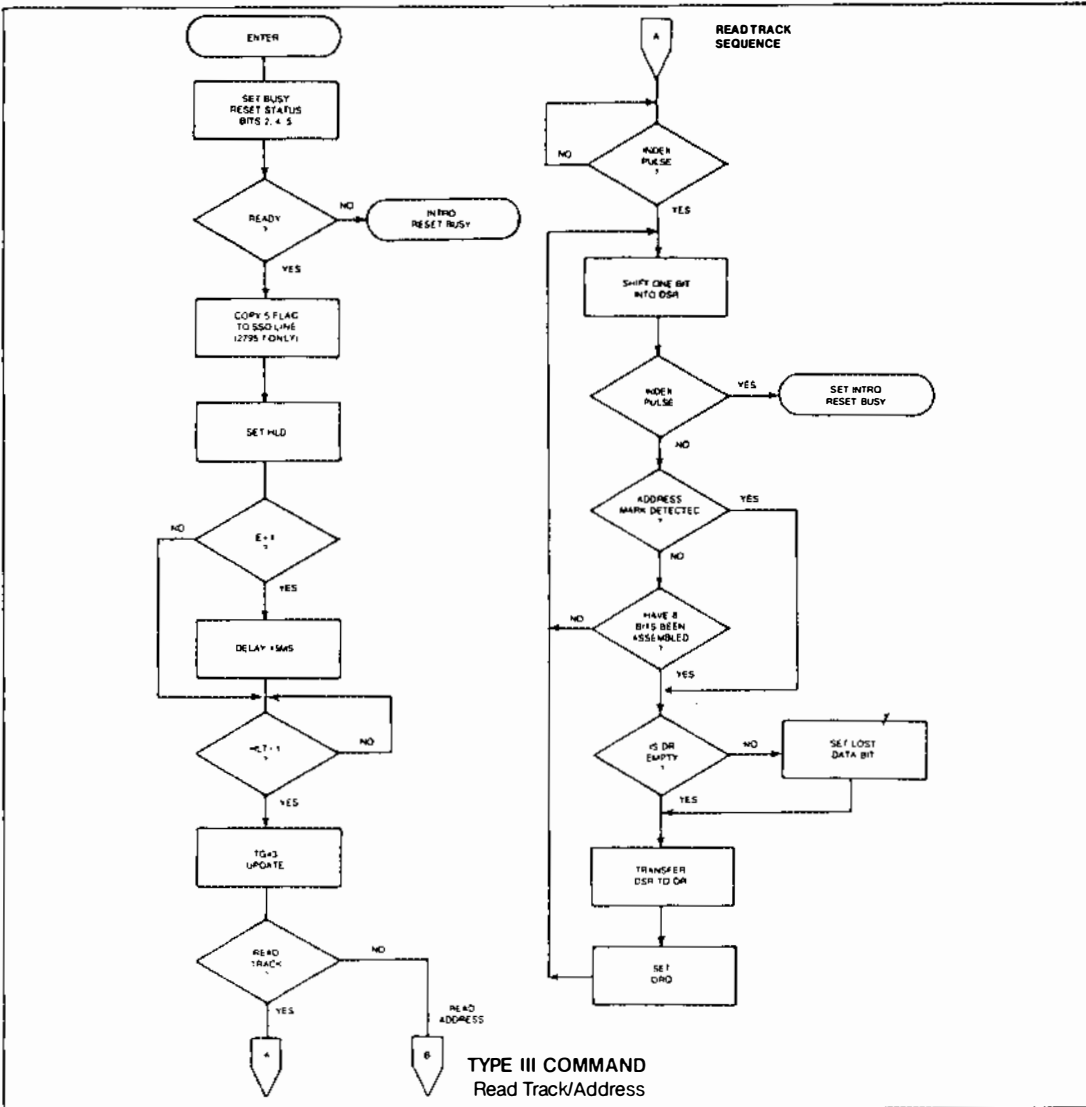
The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit

reset.

The lower four bits of the command determine the conditional interrupt as follows:

- I₀ = Not-Ready to Ready Transition
- I₁ = Ready to Not-Ready Transition
- I₂ = Every Index Pulse
- I₃ = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I₃ - I₀) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I₃ - I₀ are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate

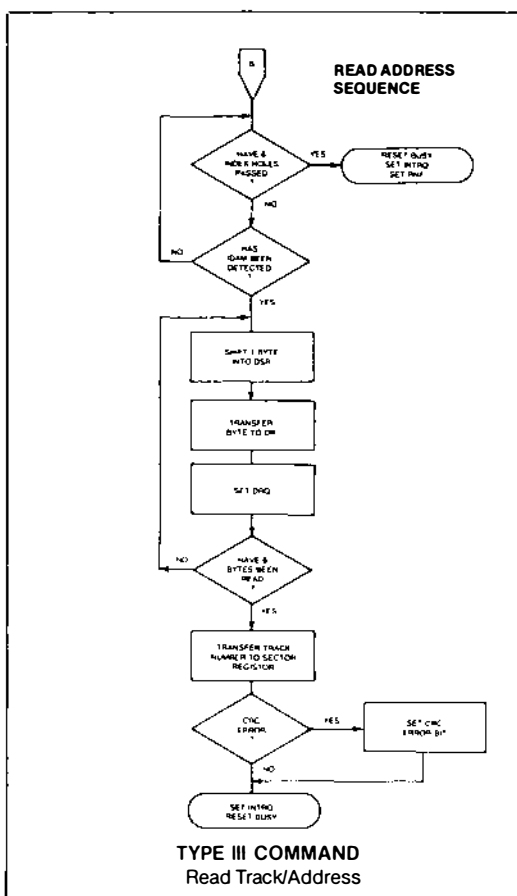


interrupt condition ($I_3 = 1$), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition ($I_1 = 1$) and the Every Index Pulse ($I_2 = 1$) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μ s	6 μ s
Write to Command Reg.	Read Status Bits 1-7	28 μ s	14 μ s
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES

40
6
1
1 26
6
1
1
1
1
1
11
6
1
128
1
27
2472

1. Write brack
2. Continue wr
3. A '00' optio

IBM SYSTEM 3
256 BYTES/SECTOR
Shown below
bytes/sector. In

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00) ³
6	00
1	FC (Index Mark)
1	FF (or 00)
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247 ²	FF (or 00)

1. Write bracketed field 26 times
2. Continue writing until 279X interrupts out.
Approx. 247 bytes.
3. A '00' option is allowed.

IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

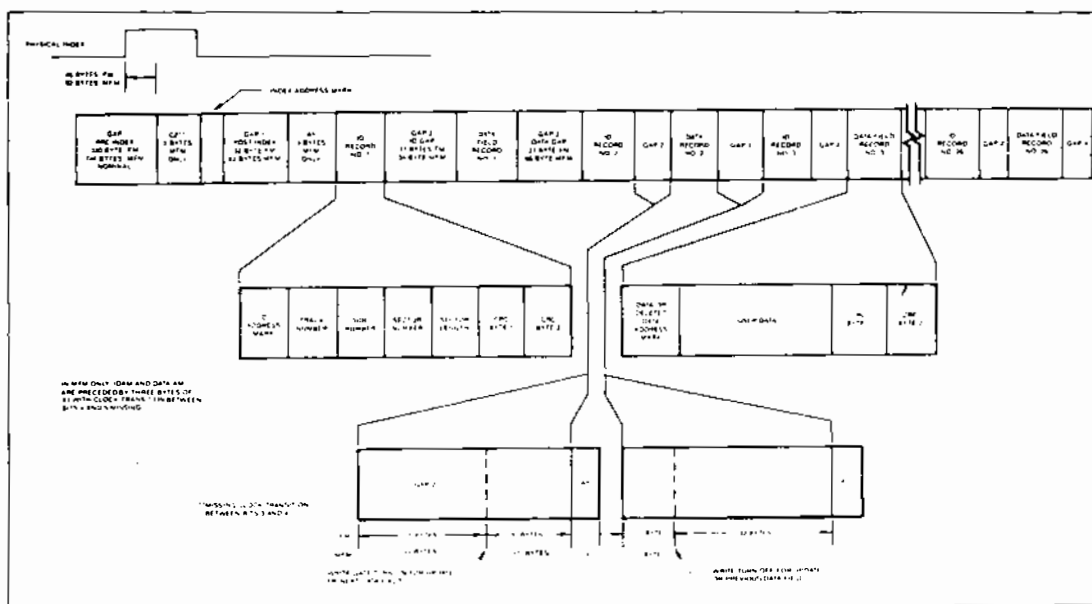
Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must

issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRC's written)
54	4E
598 ^{**}	4E

* Write bracketed field 26 times

** Continue writing until 279X interrupts out.
Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

- 1) Sector size must be 128, 256, 512 or 1024 bytes.
- 2) Gap 2 cannot be varied from the IBM format.
- 3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
.	6 bytes 00	12 bytes 00
.		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

* Byte counts must be exact.

** Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage to any input with

respect to $V_{SS} = +7$ to $-0.5V$

Operating temperature = $0^{\circ}C$ to $70^{\circ}C$

Storage temperature = $-55^{\circ}C$ to $+125^{\circ}C$

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

OPERATING CHARACTERISTICS (DC)

$T_A = 0^{\circ}C$ to $70^{\circ}C$, $V_{SS} = 0V$, $V_{CC} = +5V \pm .25V$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	$I_O = -100\mu A$
V_{OL}	Output Low Voltage			0.45	V	$I_O = 1.6 mA$
V_{OHP}	Output High PUMP	2.2			V	$I_{OP} = -1.0 mA$
V_{OLP}	Output Low PUMP			0.2	V	$I_{OP} = +1.0 mA$
P_D	Power Dissipation			.75	W	All Outputs Open
R_{PU}	Internal Pull-up*	100		1700	μA	$V_{IN} = 0V$
I_{CC}	Supply Current		70	150	mA	All Outputs Open

* Internal Pull-up resistors on PINS 1, 17, 19, 22, 36, 37 and 40. Also pin 25 on 2791 and 3.

TIMING CHARACTER

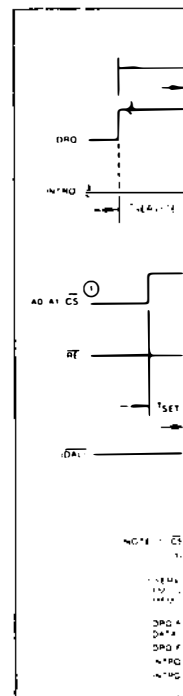
$T_A = 0^{\circ}C$ to $70^{\circ}C$, V_{SS}

READ ENABLE TIMING

SYMBOL	
TSET	Setu
THLD	Holc
TRE	RE F
TDRR	DRC
TIRR	INTF
TDACC	Data
TDOH	Data

WRITE ENABLE TIMING

SYMBOL	
TSET	Setu
THLD	Holc
TWE	WE
TDRR	DRC
TIRR	INTI
TDS	Data
TDH	Data



RE

TIMING CHARACTERISTICS

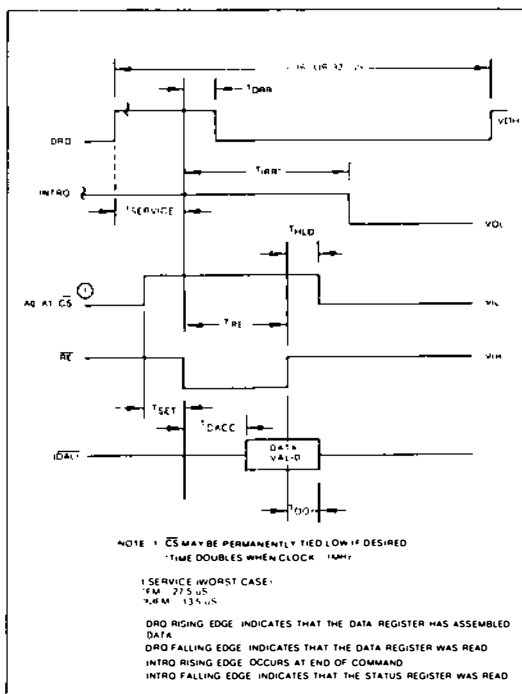
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{CC} = +5\text{V} \pm .25\text{V}$

READ ENABLE TIMING

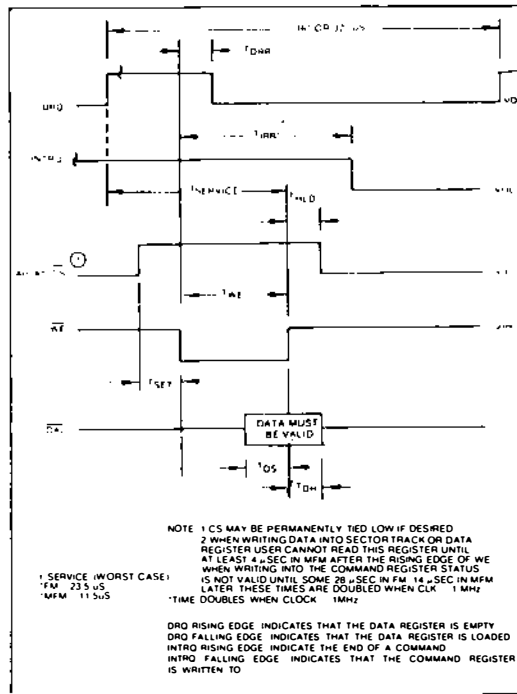
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{RE}$	50			nsec	$C_L = 50\text{ pf}$
T_{HLD}	Hold ADDR & CS from $\overline{RE}$	10			nsec	
T_{RE}	$\overline{RE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{RE}$		100	200	nsec	See Note
T_{IRR}	INTRQ Reset from $\overline{RE}$		500	3000	nsec	
T_{DACC}	Data Valid from $\overline{RE}$		100	200	nsec	
T_{DOH}	Data Hold From $\overline{RE}$	20		150	nsec	$C_L = 50\text{ pf}$

WRITE ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{WE}$	50			nsec	See Note
T_{HLD}	Hold ADDR & CS from $\overline{WE}$	10			nsec	
T_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{WE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{WE}$		500	3000	nsec	
T_{DS}	Data Setup to $\overline{WE}$	150			nsec	
T_{DH}	Data Hold from $\overline{WE}$	50			nsec	



READ ENABLE TIMING



WRITE ENABLE TIMING

WD279X-02

INPUT DATA TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T _{PW}	Raw Read Pulse Width	100	200		nsec	
T _{BC}	Raw Read Cycle Time	1500	2000		nsec	

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)(NO WRITE PRECOMPENSATION)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T _{WP}	Write Data Pulse Width	400	500	600	nsec	FM
		200	250	300	nsec	MFM
T _{WG}	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
T _{WF}	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM

MISCELLANEOUS TIMING:

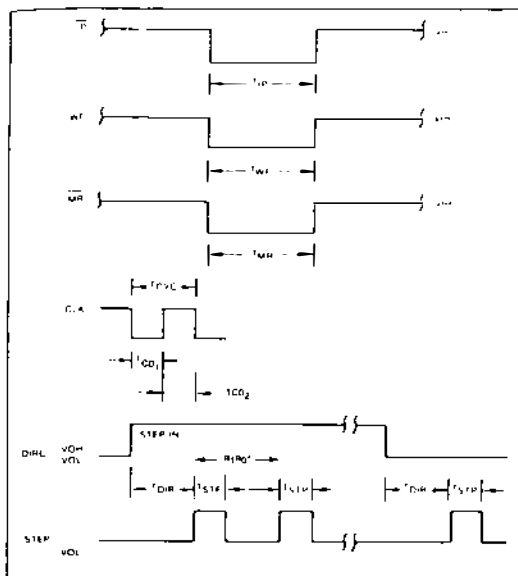
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T _{CD1}	Clock Duty (low)	230	250	20000	nsec	
T _{CD2}	Clock Duty (high)	230	250	20000	nsec	
T _{STP}	Step Pulse Output	2 or 4			μsec	See Note
T _{DIR}	Dir Setup to Step		12		μsec	± CLK ERROR
T _{MR}	Master Reset Pulse Width	50			μsec	
T _{IP}	Index Pulse Width	10			μsec	See Note
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
	Precomp Adjust.	100		300	nsec	MFM
WPW	Write Data Pulse Width	200	300	400	nsec	Precomp = 100 nsec
						MFM
WPW	Write Data Pulse Width	600	900	1200	nsec	Precomp = 300 nsec
						MFM
VCO	Free Run Voltage Controlled Oscillator. Adjustable by ext. capacitor on Pin 26	6.0	4.0		MHz	Cext = 0
	Pump Up + 25%	5.0			MHz	Cext = 35 pf
VCO	Pump Down - 25%			3.0	MHz	PU = 2.2V
						Cext = 35 pf
VCO	5% Change V _{CC}	3.8		4.2	MHz	Cext = 35 pf
	T _A = 75°C	3.5			MHz	Cext = 35 pf
Cext	Adjustable external capacitor	20	45	100	pf	VCO = 4.0MHz
						nom
RCLK	Derived read clock = VCO ÷ 8, 16, 32					VCO = 4.0MHz
			500		KHz	DDEN = 0
						5/8 = 1
			250		KHz	DDEN = 0
						5/8 = 0
			250		KHz	DDEN = 1
						5/8 = 1
			125		KHz	DDEN = 1
						5/8 = 0
PU/DON	PU/PD time on (pulse width)			250	ns	MFM
				500	ns	FM

* FROM STEP

BIT	AI
S7	NOT
S6	WRIT
	PRO
S5	HEAI
S4	SEEF
S3	CRC
S2	TRAC
S1	INDE
S0	BUS

STATUS FOR

BIT NAME
S7 NOT RE
S6 PROTEC
S5 HEAD L
S4 SEEK EF
S3 CRC ERI
S2 TRACK C
S1 INDEX
S0 BUSY

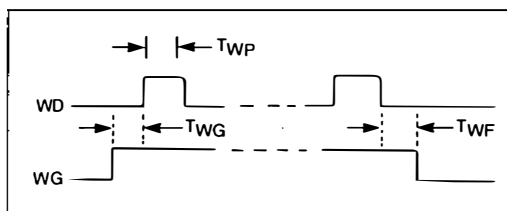


MISCELLANEOUS TIMING

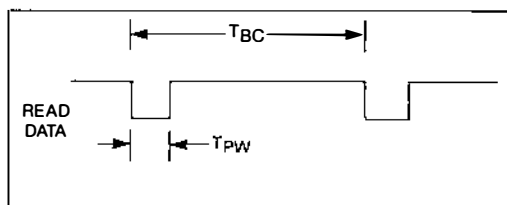
*FROM STEP RATE TABLE

NOTES:

1. Times double when clock = 1 MHz.
2. Output timing readings are at $V_{OL} = 0.8v$ and $V_{OH} = 2.0v$.



WRITE DATA TIMING



READ DATA TIMING

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TROO input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

SUMMARY OF ADJUSTMENT PROCEDURE

WRITE PRECOMPENSATION

- 1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
- 2) Strobe $\overline{\text{MR}}$ (Pin 19).
- 3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
- 4) Observe pulse width on WD (Pin 31).
- 5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
- 6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

DATA SEPARATOR

- 1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
- 2) Strobe $\overline{\text{MR}}$ (Pin 19). Insure that $\overline{\text{S}}/\overline{\text{8}}$, and $\overline{\text{DDEN}}$ are set properly.
- 3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
- 4) Observe Pulse Width on TG43 (Pin 29).
- 5) Adjust RPW (Pin 18) for 1/8 of the read clock (250ns for 8" DD, 500ns for 5 1/4" DD, etc.).
- 6) Observe Frequency on DIRC (Pin 16).
- 7) Adjust variable capacitor on VCO pin for Data Rate (500 KHz for 8" DD, 250 KHz for 5 1/4" DD, etc.).
- 8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}} = 1$ whenever a master reset pulse is applied.

INTRODUCTI

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A1 - A0		
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0 1	Tr	
1 0	S	
1 1	D	

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WESTERN DIGITAL

WD279X-02 Floppy Disk Formatter/Controller

Family Application Notes

WD279X-02

INTRODUCTION

In an effort to simplify Floppy Diskette interfacing, Western Digital has been constantly improving the LSI Controller/Formatter, the most recent of which is the WD279X Family of LSI controller devices, incorporating advanced technology to include controller, Write Precompensation and Analog Phase Lock Loop in a single 40 pin dual-in-line package. With this package we can now offer the designer the simplest ever interfacing option.

The family consists of four members, WD2791, WD2793, WD2795 and WD2797. WD2791 and WD2793 offer internal clock divide in true and inverted data bus. The WD2795 and WD2797 offer internal side select. The family supports both 5 1/4" and 8" Diskette Drives and both single and double density.

HOST INTERFACING

The LSI Diskette Controller has been developed to ease the interfacing of Processor to Disk Device. The Host interfacing with WD279X Family is accomplished with minimum external devices via an 8 bit Bi-directional bus, read/write controls, register select lines and optional control line for chip select, 5 1/4" or 8" select, enable mini floppy, double density enable. The basic operation at the controller is accomplished by selecting the device via (CS) chip select line, enabling selection of one of the five internal registers (Figure 1).

A1 - A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

Figure 1.

Each time a command is issued to the WD279X, the busy bit is set and INTRQ (Interrupt Request) line is reset. The user has the option of testing for the busy bit or polling INTRQ to determine if command has been completed.

The busy bit will be reset whenever the WD279X is idle and awaiting a new command. The INTRQ line once set, can only be reset by reading of the status register or issuing a new command.

The A0, A1 Lines used for register selections can be configured at the CPU in a variety of ways. These

lines may actually tie to CPU addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6250, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the WD279X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μ s	6 μ s
Write to Command Reg.	Read Status Bits 1-7	28 μ s	14 μ s
Write Any Register	Read From Diff. Register	0	0

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2 MHz (8" drive) or 1 MHz (5 1/4" drive) with 50% duty cycle. Accuracy should be +1% (crystal source) since all internal timing, including stepping rates, are based upon this clock, or a single 2 MHz CLK on WD2791 and WD2793 since ENMF line will internally divide CLK.

The $\overline{MR}$ or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The WD179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TR00}$ line to go active low. This line should be connected to the drive's $\overline{TR00}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.

The 5/8 Line selects internal VCO frequency to be used with 5 1/4" or 8" drives.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the

drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the WD279X. Inputs to the WD279X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed -0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\bar{IP}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. sensor that informs the WD279X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open," Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The WD279X will look at the ready signal prior to executing READ/WRITE commands. READY is not inspected during any Type 1 commands. All type 1 commands will execute regardless of the Logic Level on this Line.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the WD279X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_{1r0} field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the WD279X terminated operations, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the WD279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r_{1r0} field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the WD2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

For write operations, the WD279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the WD279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DE

The WD279X w
mand words sh
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Whenever a cor
status bit is set.

Table 1. COMM

A. Commands for

Type	Command
I	Restore
I	Seek
I	Step
I	Step-in
I	Step-out
II	Read Sector
II	Write Sector
III	Read Address
III	Read Track
III	Write Track
IV	Force Interr

COMMAND DESCRIPTION

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, and

interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Command types are summarized in Table 1 and Table 2.

WD279X-02

Table 1. COMMAND SUMMARY

A. Commands for Models: 2791, 2793

B. Commands for Models: 2795, 2797

Type Command	Bits								Bits							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I Restore	0	0	0	0	h	V	r1	r0	0	0	0	0	h	V	r1	r0
I Seek	0	0	0	1	h	V	r1	r0	0	0	0	1	h	V	r1	r0
I Step	0	0	1	T	h	V	r1	r0	0	0	1	T	h	V	r1	r0
I Step-in	0	1	0	T	h	V	r1	r0	0	1	0	T	h	V	r1	r0
I Step-out	0	1	1	T	h	V	r1	r0	0	1	1	T	h	V	r1	r0
II Read Sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II Write Sector	1	0	1	m	S	E	C	a0	1	0	1	m	L	E	U	a0
III Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV Force Interrupt	1	1	0	l1	l3	l2	l1	l0	1	1	0	1	l3	l2	l1	l0

Table 2. FLAG SUMMARY

Command Type	Bit No(s)		Description																				
I	0, 1	r1 r0 = Stepping Motor Rate See Table 3 for Rate Summary																					
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track																				
I	3	h = Head Load Flag	h = 0, Load head at beginning h = 2, Unload head at beginning																				
I	4	T = Track Update Flag	T = 0, No update, T = 1, Update track register																				
II	0	a0 = Data Address Mark	a0 = 0, FB (DAM) a0 = 1, F8 (deleted DAM)																				
II & III	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare																				
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1																				
II & III	2	E = 15 MS Delay	E = 0, No 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)																				
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1																				
II	3	L = Sector Length Flag	<table><tr><th colspan="5">LSB's Sector Length in ID Field</th></tr><tr><th></th><th>00</th><th>01</th><th>10</th><th>11</th></tr><tr><td>L = 0</td><td>256</td><td>512</td><td>1024</td><td>128</td></tr><tr><td>L = 1</td><td>128</td><td>256</td><td>512</td><td>1024</td></tr></table>	LSB's Sector Length in ID Field						00	01	10	11	L = 0	256	512	1024	128	L = 1	128	256	512	1024
LSB's Sector Length in ID Field																							
	00	01	10	11																			
L = 0	256	512	1024	128																			
L = 1	128	256	512	1024																			
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records																				
IV	0-3	Ix = Interrupt Condition Flags I0 = 1 Not Ready To Ready Transition I1 = 1 Ready To Not Ready Transition I2 = 1 Index Pulse I3 = 1 Immediate Interrupt, Requires A Reset* I3-I0 = 0 Terminate With No Interrupt (INTRQ)																					

*NOTE: See Type IV Command Description for further information.

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FEATURES

- DIRECT INTER
- ELIMINATES
- DATA SEPARA
- WRITE PRECC
- VFOE/WF DEN
- PROGRAMMA
- 8" OR 5.25" C
- ALL INPUTS /
- SINGLE +5V

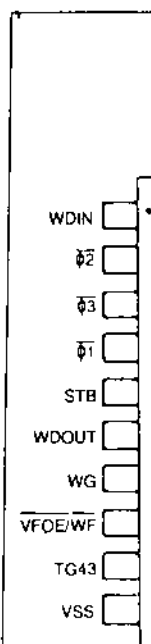


Figure 1 W

AMPEX

AMPEX CORPORATION

REDWOOD CITY, CALIFORNIA USA