

HP 9000 Series 800 Computer Systems



Hardware Technical Data

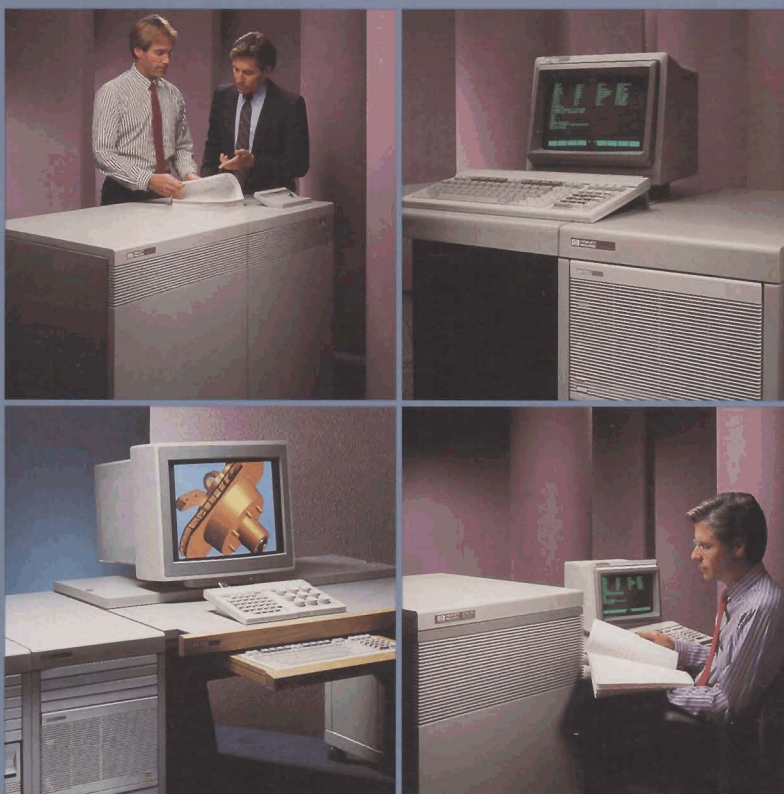


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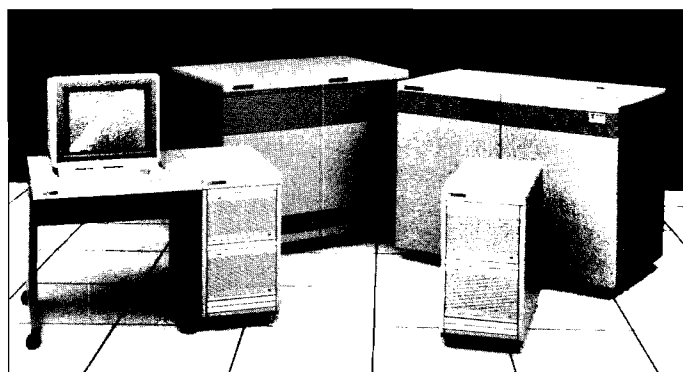


HP Precision Architecture

HP Precision Architecture is a reduced complexity architecture which provides the framework for Hewlett-Packard computer systems for the 1990's and beyond. Precision Architecture is an embodiment and extension of Reduced Instruction Set Computer (RISC) architectural principles. Processor hardware is optimized for the simple, often executed functions, leaving implementation of more complex functions to software. Instructions are executed directly in hardware in a single, fast CPU cycle, without the overhead and complexity of a microcoded control store. Support of a simple instruction set allows previous HP architectures to be emulated very effectively, providing full software compatibility and thus a convenient growth path to Precision Architecture systems. Full 48-bit and 64-bit virtual addresses are supported, representing a significant expansion over the addressability of typical 32-bit systems. A key design objective was scalability, such that cost-effective solutions can be provided from desktop systems all the way through systems with the power of today's mainframes. Provisions have been made for multiprocessors and special function coprocessors, as well as redundant, high availability features. Coupled with support for high-speed floating point calculations, HP Precision Architecture is ideally suited to providing cost-effective, high performance commercial and technical computing solutions.

Features

- Reduced instruction set
- 32-bit instructions, fixed format
- 48-bit or 64-bit virtual addressing
- Hardwired, single-cycle instruction execution
- Register intensive operation
- 32 general purpose registers
- 32 control registers
- 8 Space Registers
- Only LOADs and STOREs access memory
- Hardware support for floating point and decimal calculations
- Demand-Paged memory management scheme
- Multiprocessors and special function coprocessors
- Memory-Mapped I/O



RISC Motivations

Many computer architectures which have evolved over the last twenty years have tended towards increasing system complexity. System architectures which provide large, complex instruction sets are loosely called CISCs (Complex Instruction Set Computers). CISCs typically utilize a micro-coded control store to provide instruction set support for high level languages and complex functions, such that instructions require multiple CPU cycles to execute.

Extensive research in industry and at leading universities has shown, however, that CISCs spend the great majority of the time executing simple instructions such as ADD, LOAD, STORE, and BRANCH. The more complex instructions, which necessitate a greater level of processor complexity, are utilized relatively infrequently. The net result with architectures that support large, complex instruction sets is that a performance penalty is often encountered even for the simple, often-executed instructions, due to the overhead of additional instruction decoding and control hardware. This overhead can increase CPU cycle time, and can negate any advantage of providing an instruction set which directly supports more complex functions.

These findings led to the concept of reduced complexity RISC architectures. The key RISC concept is to optimize the system to execute simple, often-used instructions directly in hardware in a single, fast CPU cycle. Extensions of RISC concepts have been embodied in HP Precision Architecture to provide a flexible, expandable architecture which maximizes performance realized from a given semiconductor technology, and achieves a given level of performance at a significantly lower cost than other systems.

Instruction Set

HP Precision Architecture defines 140 instructions. Each is 32-bits long and has a fixed format. The instruction set directly implements only simple functions in order to minimize processor complexity.

Memory Reference Instructions

Data in memory is referenced only via Load and Store instructions. Operands required for a given operation must first be brought into a CPU register with a Load instruction, and the result of the calculation must be explicitly moved to memory via a Store instruction. Accessing memory with only Load/Store instructions, coupled with support for a relatively large number of CPU registers, allows for frequently required operands to be held in the CPU. A performance increase can thus be realized, as the number of accesses to cache and main memory are minimized.

Arithmetic and Logical Instructions

The arithmetic and logical functions provided by the instruction set are limited to relatively simple functions, with appropriate primitives provided for common operations. For example, Shift-and-Add instructions accelerate integer multiplication, and Extract/Deposit instructions efficiently support bit-manipulation functions utilized by high-level languages. More complicated functions are implemented by executing a sequence of simple instructions.

Decimal Arithmetic Support

Primitives such as the *Decimal Correct* and *Unit Add Complement* instructions allow for packed and unpacked decimal addition to be performed with the binary *Add* instruction. Packed, unpacked, and zoned decimal operations can easily be supported by compilers.

Floating Point Instructions

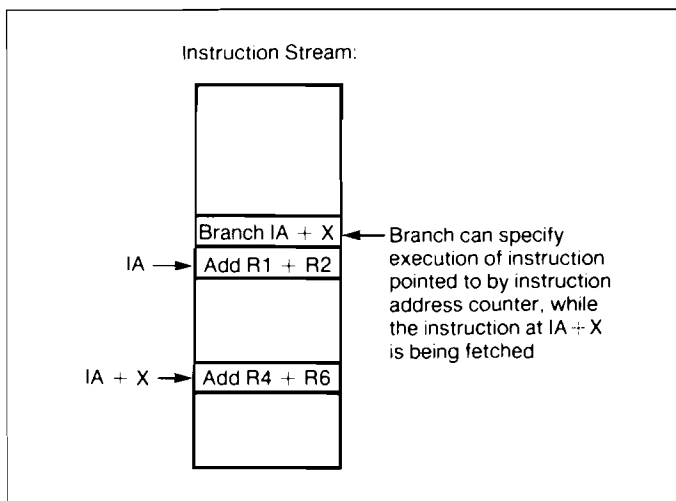
Floating point instructions are available to support single-precision (32-bit), double-precision (64-bit) and quadruple-precision (128-bit) arithmetic operations. Floating point instructions can either be executed directly in hardware by a coprocessor, or can be emulated in software. With a floating point coprocessor, floating point calculations can be performed while the CPU continues to execute in parallel.

Branch Instructions

Conditional branch instructions perform an operation, evaluate a branch condition, and perform the branch (if appropriate) in a single instruction. The need for some branch sequences is eliminated altogether as most computational instructions can specify conditional execution of the next instruction, allowing such common functions as boolean value generation to be performed in a simple, non-branching instruction sequence.

Single-Cycle Instruction Execution

Instructions are executed directly in hardware, and typically will execute in only one CPU cycle. Branch instructions and Load/Store instructions may require more than one cycle to execute, but are implemented and scheduled such that effective execution rates approaching one cycle per instruction are achieved. A delayed branch capability allows branch instructions to specify that the next sequential instruction be executed, and compilers schedule instructions to utilize this capability when possible. Thus the "dead" cycle typically encountered for taken branches on other systems can often be avoided. Similarly, Load instructions can be scheduled such that useful processing of other instructions is done while the data is being fetched. To avoid pipeline delays, instructions which require the data being loaded are not scheduled for execution, if possible, until the data is available in a CPU register.



Delayed-Branch Capability

Data Types

Integers

HP Precision Architecture supports 16-bit and 32-bit integers, either signed or unsigned. Signed integers are in 2's complement form. To help minimize processor complexity, halfword (16-bit) integers must be aligned at even byte addresses, and 32-bit integers must be aligned on a word boundary.

Characters

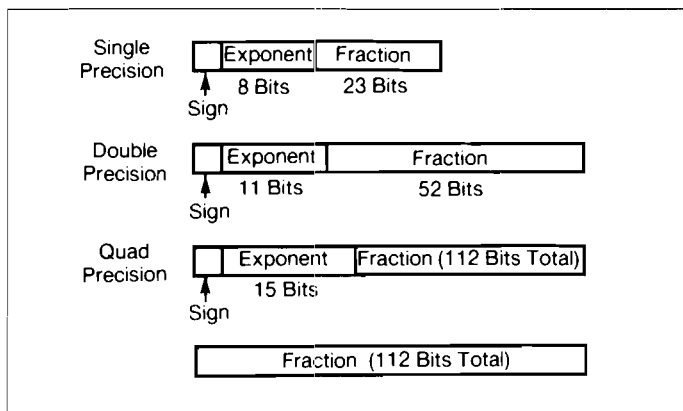
Characters are stored as 8-bit quantities, conforming to the ASCII standard for values 0 through 127, and HP's 8-bit extended Roman-8 character set for values 128 through 255.

Decimal Data

Both packed and unpacked decimal data representations are supported. Packed decimal data is always aligned on a word boundary, and consists of 7, 15, 23, or 31 Binary Coded Decimal digits.

Floating Point Operands

Single, Double, and Quadruple-word floating point operands are represented in accordance with the ANSI/IEEE 754-1985 standard. Single-precision floating point numbers must be aligned on word boundaries, and Double and Quadruple-precision numbers must be aligned on double-word boundaries.



Floating Point Operand Format

CPU Register Set

HP Precision Architecture specifies register-intensive operation. Calculations are performed only between high-speed CPU registers, or between a CPU register and a constant held in the instruction. Register-intensive operation allows for simplified data and control paths and increased processor performance. Optimizing compilers allocate the most frequently used variables to General Purpose Registers to minimize the number of memory references.

General Purpose Registers

There are 32 available General Purpose Registers for holding operands and results of processor computations. All General Purpose Registers are 32-bits wide.

Control and Status Registers

There are 32 control and status registers in the CPU, which are used for interrupt processing, virtual memory access protection, and other system functions. CPU status is maintained in the 32-bit Processor Status Word (PSW), which reflects the state of key CPU flags and status bits.

Space Registers

Eight Space Registers in the processor are used to specify up to eight possibly different 4GB virtual spaces that can be utilized for a given operation. These registers can hold 16-bit or 32-bit space identifiers, with the space identifier length chosen dependent upon the amount of addressability appropriate for a given system. Five of these registers can be used directly by application programs.

Instruction Address Registers

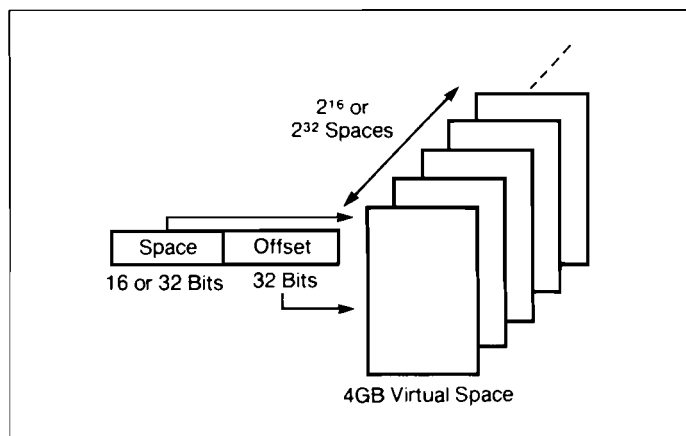
Two CPU registers are used to point to the next instruction to be executed. The Instruction Address Space Register (IA Space) points to the 4GB space which holds the next instruction. The Instruction Address Offset Register (IA Offset) points to the location, within that space, which holds the instruction. Each of these registers is, in fact, a two-element queue, reflecting architectural visibility of the next two instructions being processed in the pipeline.

Virtual Addressing

HP Precision Architecture provides for support of 48-bit virtual addresses, representing a significant expansion over the virtual addressability of typical 32-bit systems. The instruction set additionally provides direct access to physical memory locations, and low-cost systems will have the option of providing only physical addressing if appropriate. The smallest addressable quantity is a byte.

Virtual Memory Management

Virtual Memory is organized as a set of linear spaces, with each space 4GB in length. Spaces are further divided into fixed length 2KB pages, each of which can hold either code, data or both. Space Registers point to the virtual space to be accessed, and the specific location within that space is specified by a 32-bit quantity called the *byte offset*. Multiple simultaneous spaces are supported. Code can span spaces, and a single data structure can be up to a full 4GB space in length.



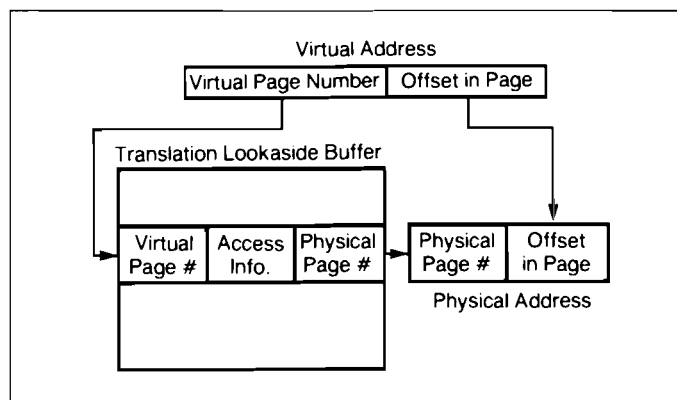
Virtual Memory Organization

Memory Mapped I/O

HP Precision Architecture incorporates a memory-mapped I/O scheme, whereby I/O operations are initiated and controlled via a series of Load/Store instructions to reserved virtual or real space locations. This allows I/O devices to efficiently utilize the same access protection mechanisms as code and data. No I/O-specific instructions are required for performing I/O. Coupled with other I/O subsystem features such as DMA Chaining, which allows multiple transactions to be processed without CPU intervention, I/O operations on Precision Architecture systems carry less overhead and are streamlined for increased I/O performance.

Virtual Address Translation

Virtual Addresses are translated to physical addresses using Translation Lookaside Buffer (TLB) hardware in the processor. TLBs contain translations for recently accessed virtual pages. They can be organized as two logical TLBs, one for code and one for data, or can be combined into a single TLB.



Virtual Address Translation

Virtual Memory Access Protection

The TLB hardware supports protection mechanisms to assure that the currently executing process can perform only the code, data, or I/O accesses for which it is authorized. Included in the access checking mechanisms are four privilege levels. Protection parameters are associated with each page, and these parameters define what privilege level is required to access that page, as well as what types of accesses are permitted. For each requested access, these privilege parameters are checked against the privilege level of the currently executing process, to ensure that the process has sufficient authorization to perform that access.

Caches

Processor caches may be organized as a single, unified cache, holding both instructions and data, or there may be separate instruction and data caches. So that the machine cycle time can be minimized, the I/O subsystems do not interface to the cache, and it is the responsibility of software to update main memory contents with any modified cache contents before launching a DMA I/O operation. Instruction caches are read only, as code is typically non-modifiable.

Coprocessors

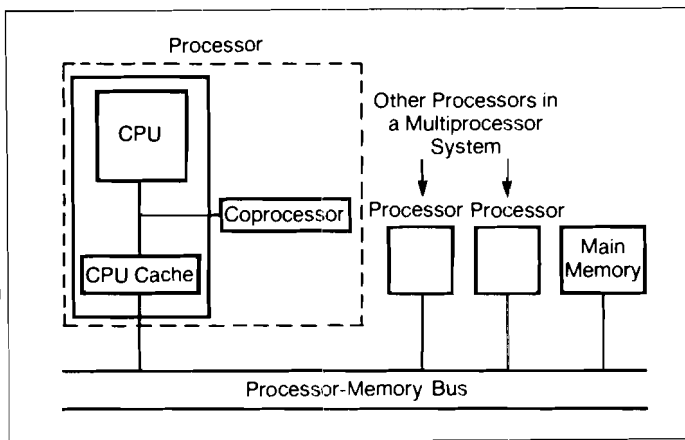
HP Precision Architecture has provisions for integration of coprocessors which share the main processor caches. Coprocessors are controlled by a subset of the instruction set, and are typically utilized to enhance performance of special functions, for example, high performance floating point calculations. Coprocessors contain their own register set which may directly interface with the cache.

Attached Processors

Provisions are made for attached processors, which interface to the system hierarchy at the memory bus level, and typically have their own register set and local cache(s). Attached processors can provide such functions as I/O processing or vector processing. They may execute either the same instruction set, or a different instruction set, as the main processor.

Multiprocessors

Multiprocessors are identical, attached processors. They can be configured either in parallel, to increase performance via distribution of the system workload, or can be configured redundantly to provide fault tolerance. Each processor has its own register set and local cache storage, and executes the entire instruction set. Provisions are made for development of tightly-coupled, symmetric multiprocessor systems.



Coprocessors and Attached Processors

Optimizing Compilers

Reduced complexity architectures are ideal for optimizing compilers, and compiler optimization is required for the highest performance on such machines. The optimizing compilers utilized with HP Precision Architecture systems maximize processor efficiency in a number of ways. For example, scheduling instructions to make the most efficient use of the available cycle after a taken Branch. By allocating the most frequently accessed operands in an instruction stream to CPU general purpose registers, the number of references to cache and main memory is minimized. Compilers used with Precision Architecture systems also provide features to correct some inefficient high-level language programming practices. For example, computations within a loop that produce the same result for each iteration can be moved outside of the object code loop, and other duplicate computations in a program can be eliminated during object code generation.

VLSI

Precision Architecture allows for systems to be implemented in a wide variety of semiconductor technologies. With a reduced amount of circuitry required to implement processor functions, maximum benefits can be realized from Very Large Scale Integrated (VLSI) components. Processor performance can be maximized by placing an entire CPU on-chip, thus keeping signal delays short and allowing CPU cycle time to be decreased. With further integration, such as placing CPU, caches, and TLBs on-chip, code and data access times can also be minimized, providing for additional performance gains. The performance advantages and low cost of VLSI implementations allow cost effective high performance systems, as well as powerful, low-cost office systems and workstation products.

Instruction Set Listing

Memory Reference Instructions

Load Word
Load Halfword
Load Byte
Load Word Indexed
Load Halfword Indexed
Load Byte Indexed
Load Word Short
Load Halfword Short
Load Byte Short
Load Word and Modify
Load Word Absolute
Load Word Absolute Short
Load Offset
Load and Clear Word Indexed
Load and Clear Word Short
Store Word
Store Halfword
Store Byte
Store Word Short
Store Halfword Short
Store Byte Short
Store Word and Modify
Store Word Absolute Short
Store Bytes Short

Unconditional Branches

Branch and Link
Gateway
Branch and Link Register
Branch Vectored
Branch External
Branch and Link External

Conditional Branches

Move and Branch
Move Immediate and Branch
Compare and Branch if True
Compare and Branch if False
Compare Immediate and Branch if True
Compare Immediate and Branch if False
Add and Branch if True
Add and Branch if False
Add Immediate and Branch if True
Add Immediate and Branch if False
Branch on Variable Bit
Branch on Bit

Arithmetic/Logical Instructions

Add
Add Immediate
Add Immediate Left
Load Immediate Left
Add Logical
Add and Trap on Overflow
Shift One and Add
Shift Two and Add
Shift Three and Add
Shift One and Add Logical
Shift Two and Add Logical
Shift Three and Add Logical
Shift One, Add, and Trap on Overflow
Shift Two, Add, and Trap on Overflow
Shift Three, Add, and Trap on Overflow
Add with Carry
Add with Carry and Trap on Overflow
Subtract
Subtract from Immediate
Subtract and Trap on Overflow
Subtract Immediate and Trap on Overflow*
Subtract with Borrow
Subtract with Borrow and Trap on Overflow
Subtract and Trap on Condition
Subtract and Trap on Condition or Overflow
Divide Step
Compare and Clear
Inclusive OR
Exclusive OR
AND
AND Complement
Unit XOR
Unit Add Complement
Unit Add Complement and Trap on Condition
Decimal Correct
Intermediate Decimal Correct
Add Immediate and Trap on Overflow
Add Immediate and Trap on Condition
Add Immediate, Trap on Condition or Overflow
Compare Immediate and Clear
Variable Shift Double
Shift Double
Variable Extract Signed
Variable Extract Unsigned
Extract Signed
Extract Unsigned
Variable Deposit
Variable Deposit Immediate
Deposit
Deposit Immediate
Zero and Variable Deposit
Zero and Variable Deposit Immediate
Zero and Deposit
Zero and Deposit Immediate

System Control Instructions

Break
Return From Interrupt
Set System Mask
Reset System Mask
Load Space ID
Move to Space Register
Move to Control Register
Move from Space Register
Move from Control Register
Move to System Mask
Synchronize Caches
Probe Read Access
Probe Read Access Immediate
Probe Write Access
Probe Write Access Immediate
Load Physical Address
Load Hash Address†
Purge Instruction TLB
Purge Instruction TLB Entry
Purge Data TLB
Purge Data TLB Entry
Insert Data TLB Address
Insert Data TLB Protection
Insert Instruction TLB Address
Insert Instruction TLB Protection
Purge Data Cache
Flush Data Cache
Flush Instruction Cache
Flush Data Cache Entry
Flush Instruction Cache Entry
Diagnose

Special Function Unit Operations

Special Operation Zero†
Special Operation One†
Special Operation Two†
Special Operation Three†

Coprocessor Loads and Stores

Coprocessor Load Word Short
Coprocessor Load Word Indexed
Coprocessor Load Doubleword Short
Coprocessor Load Doubleword Indexed
Coprocessor Store Word
Coprocessor Store Indexed
Coprocessor Store Doubleword
Coprocessor Store Doubleword Indexed
Coprocessor Operation*

* Floating Point Operations Included

† Not implemented on HP 9000 Model 840

product numbers A1004A, A1005A, 9741A, 9742A

The Series 800 is the first HP 9000 family of computers to use HP Precision Architecture. Running under the HP-UX operating system, the Series 800 computers offer higher performance than the HP 9000 Series 300 or HP 1000 A900 families. Significant enhancements have been added to HP-UX to equip the operating systems for real-time super minicomputer applications. These HP-UX enhancements make the HP 9000 Series 800 family a logical extension of both the HP 9000 and the HP 1000 product lines.

The speed and capacity of the Series 800 systems makes them a good choice for scientific applications, such as those found in the defense and aerospace industries. These include electronics modeling, circuit simulations, numerical analyses, finite element analyses, signal processing, and other large software, computation intensive applications.

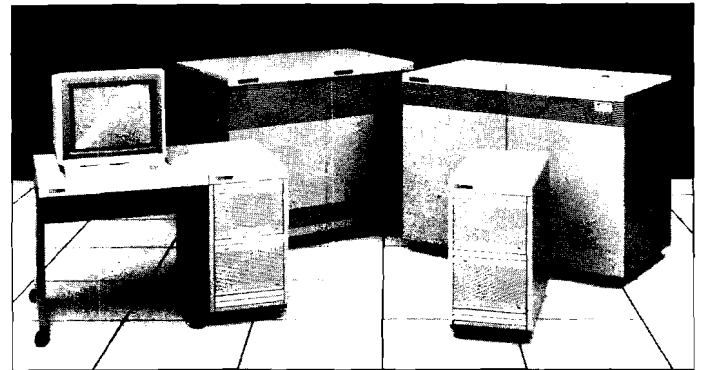
In communications applications, the Series 800 systems are excellent choices for controlling, processing, and directing data between other computers and electronic devices. The high data throughput capabilities along with the HP-UX operating system meet industry needs in many communication applications. A Series 800 system is a good fit for network management and control, telephone monitoring, message switching, navigation and satellite control.

In workstation applications, the high performance and capacity of the Series 800 address the industry's needs for improved computational capabilities and graphics performance. With this increase of power at the workstation level, the Series 800 may be used to run applications such as ME Solids Modeling, Molecular Modeling, Graphics, Architectural-Engineering-Construction (AEC), Mapping, and real-time simulation tasks.

For use in the software development environment, the Series 800 systems offer sophisticated optimizing compilers which generate clean and efficient code. Again, the large program support and fast compile speeds within the HP-UX environment makes the Series 800 the preferred system for technical users and OEMs.

System Features

- HP Precision Architecture with 32-bit word size, reduced complexity, and 48-bit virtual addressing.
- High CPU performance.
- High floating point performance.
- Expandable memory for increased system flexibility.
- Translation Lookaside Buffer for virtual-to-physical address translations.



- 4 Gigabyte virtual address space per process.
- Multi/Concurrent user capability.
- HP-UX operating system, a superset of AT&T's System V Interface Definition (Issue 2, vol. 1), SVVS (System V Verification Suite) complaint, with over 200 utilities from AT&T's System V.2 and other popular UNIX* versions, plus added enhancements, including real-time capability and Native Language Support (internationalization).
- Operating system compatibility with the HP 9000 Series 200, 300, 500 and Integral PC.
- PORT/HP-UX to assist migration of applications from RTE-A or RTE-6/VM based HP 1000 systems.
- Support for:
 - C, FORTRAN 77, and PASCAL programming with optimizing compilers.
 - ALLBASE/HP-UX network and relational database management system with IMAGE interface.
 - HPtoday for database-oriented application generation.
 - Graphics software packages based on evolving ANSI and international standards, providing upward compatibility for existing applications as well as high speed performance.
 - System Networking hardware and software products for communication with other HP 9000 systems, the HP 1000 A-Series systems, and other computer vendors.
 - ARPA/Berkeley Network Services.
- Remote console capability for invoking diagnostics and system reset.

*"UNIX is a registered trademark of AT&T in the U.S. and other countries."

HP Precision Architecture

The HP 9000 Series 800 utilizes the new reduced complexity HP Precision Architecture. The Series 800 embodies the basic principles of Reduced Instruction Set Computers and extends beyond them, including support for extended addressing, high performance Input/Output, and high speed floating point calculations. Other key characteristics of Precision Architecture include:

- Fixed-length, limited-format instruction set.
- Pipelined Instruction Execution.
- Hardwired Control (no microcode required).
- Register Intensive Operation.
- General Purpose Registers.
- Control Registers.
- Space Registers for virtual addressing.

System Organization

The system structure for the Series 800 computers are depicted in figures 1, 2, and 3. The Central System Bus provides a 32-bit data path, and can support sustained data transfer rates approximately up to 33 MB/second. The central bus (CTB) is interfaced to a 16-bit wide Channel I/O Bus via a CIO Adapter. The Channel I/O Bus supports I/O interfaces to peripheral devices and data communication links.

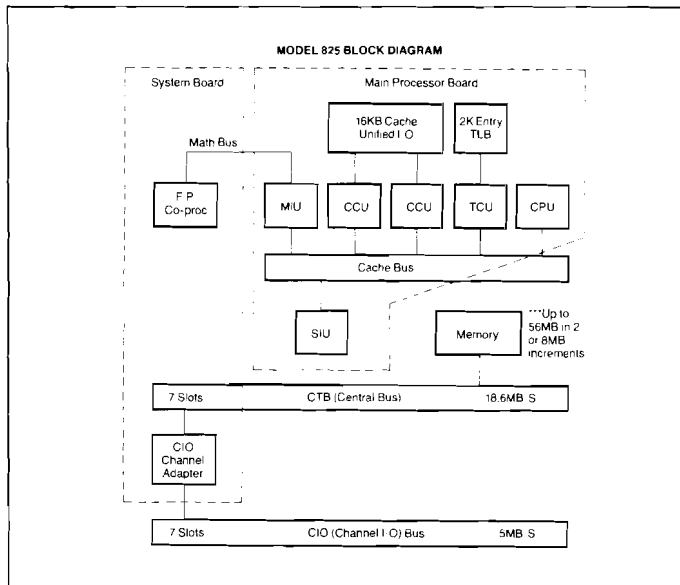


Figure 1. Model 825 System Structure

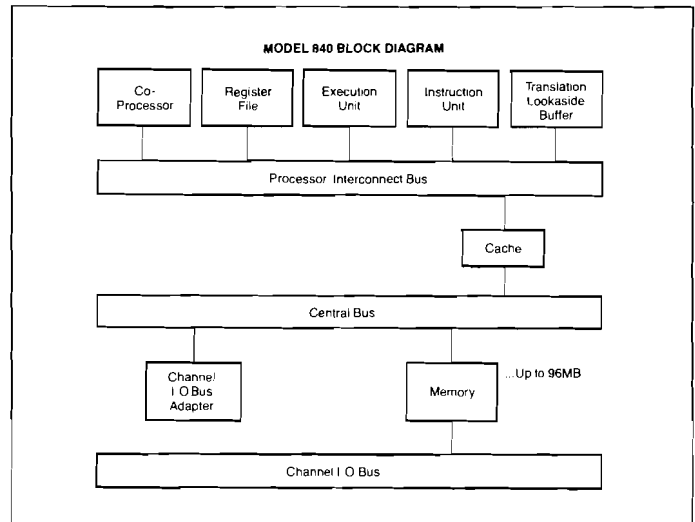


Figure 2. Model 840 System Structure

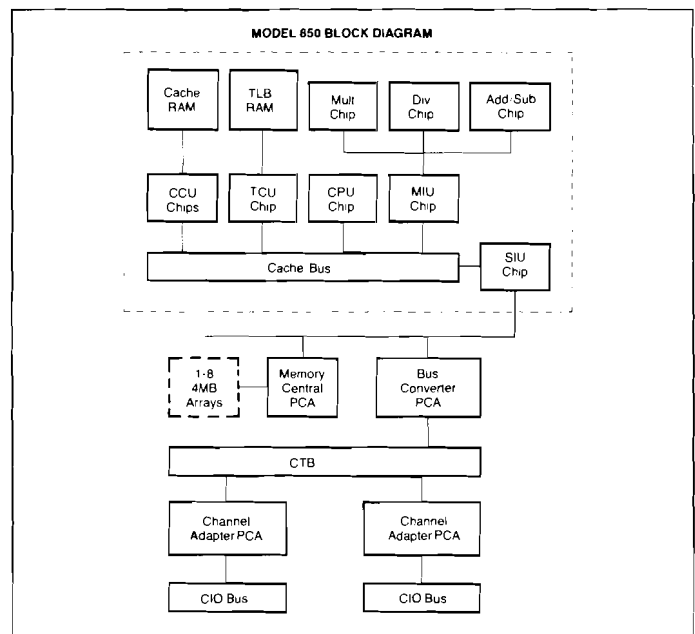


Figure 3. Model 850 System Structure

Caches

The HP 9000 Series 800 systems are implemented with cache memory. By using cache memory, instruction and data fetches are optimized for maximum efficiency and increased performance.

The cache significantly reduces memory access time by storing frequently used data and instructions. This greatly improves system performance since accessing cache memory is 10 times faster than accessing the main memory modules. Efficiency is also achieved by prefetching multiple instructions/data during a cache miss.

Instruction Pipelining

Each Series 800 system is pipelined at the instruction level, such that more than one instruction can be operated on at the same time. During the first stage the instruction is fetched from the cache and decoded. The specified function or calculation is performed during the second stage, and in the third stage the result of the calculation is saved to a CPU general purpose register.

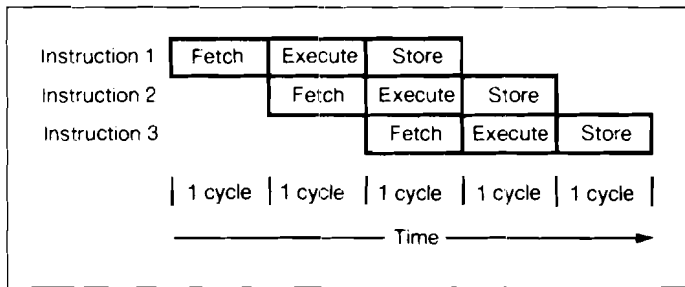


Figure 4. Instruction Pipelining

Floating Point Capability

Single-precision and double-precision floating point calculations are performed by a Floating Point Coprocessor. The additional processor set significantly decreases the time required to perform floating point calculations. Floating point calculations and CPU operations work in parallel for maximum efficiency.

Virtual Memory Management

Virtual Addresses on the Series 800 are 48 bits long, ensuring sufficient expandability to meet growing software needs. As shown in Figure 5, Virtual Memory is divided into a set of 65,536 spaces, with each space 4 GB long. Spaces are further divided into fixed length 2 KB pages, with a given page holding data, code, or both. A single data structure can be up to 1 GB long.

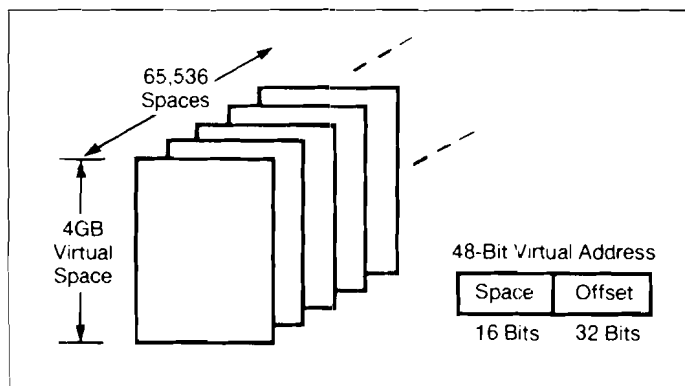


Figure 5. Virtual Memory Organization

Virtual Address Translation

Virtual-to-Physical address translation is done by Translation Lookaside Buffers (TLBs). TLBs are used to cache recently accessed virtual page translations and convert the 48-bit virtual address into a 28-bit physical address. Each system implements page-level access protection and the TLB hardware supports protection mechanisms to assure

that the currently executing process has sufficient authorization to perform requested data, code, and I/O accesses.

Memory Subsystem

Each Series 800 computer includes either 8MB or 16MB of ECC memory, expandable in different increment options. The memory subsystem uses 256K-bit, or 1M-bit dynamic RAM. Main memory is backed up such that if AC power is lost and restored within 15 minutes, the operating system is automatically restarted and processing can resume without data loss.

Single-bit errors are automatically corrected. Multi-bit errors are automatically detected, causing an interrupt. Overall, the ECC memory of the Series 800 computers guarantees high performance and high availability.

I/O Subsystem

I/O Bus

The Series 800 utilizes a general-purpose channel I/O (CIO) bus. This I/O is used for connection of peripheral devices and data communication cards. Additional slots and channels are available for each model offering greater expandability. Two interfaces, an HP-IB and a multiplexor, are included in the Basic SPU's.

The I/O Manager

The Channel I/O (CIO) Adapter interfaces the Central Bus to the CIO bus, synchronizing their differing speeds and bandwidths. The CIO Adapter manages Direct Memory Access (DMA) transfers between CIO interfaces with their associated peripherals and main memory. Because the CIO Adapter accomplishes this function with little CPU intervention, interrupting only to signal completion of the DMA transfers, it leaves the CPU free to perform other operations during I/O. Large blocks of data can be transferred to and from main memory with negligible CPU overhead.

Peripheral Connection

The Series 800 uses the following device interface cards for connection to peripheral devices or other systems:

- HP 27110B HP-IB card for discs, tape drives, printers, and plotters.
- HP 27140A Six-channel Multiplexor for terminals and other RS-232 C devices and for UUCP communication with other systems running under the UNIX operating system.
- Interface card in HP LAN/9000 Series 800 Link interface-software package for inter-system communication.
- HP 27114A Parallel Asynchronous FIFO Interface (AFI) card for miscellaneous interfacing.

NOTE: The following paragraphs briefly discuss the HP-UX operating system and other software products for the Series 800 super minicomputer system. More detailed information is provided in the HP 9000 Series 800 Software Technical Data book, HP Literature Stock Number 5953-8788.

The Operating System

The Series 800 systems support the HP-UX operating system. HP-UX is a superset of AT&T's System V Interface Definition (Issue 2, vol 1) and SVVS (System V Verification Suite) compliant. In addition, HP-UX incorporates features from U.C. Berkeley release 4.2 BSD and all non-hardware dependent utilities from AT&T's System V.2 UNIX system. HP developed extensions add significant capabilities, such as real-time functionality that includes priority ordered time and event scheduling of programs with real-time process dispatch latency for fast response.

Native Language Support

HP-UX, terminals, printers, and plotters provide facilities and options for supporting 18 different languages. Languages supported include American English, Canadian, French, Danish, Dutch, U.K. English, Finnish, German, Italian, Japanese, Greek, Turkish, Norwegian, Spanish, Swedish, Portuguese, Arabic, and Hebrew.

Graphics

The Series 800 supports several graphics packages for development of sophisticated graphics applications based on industry graphics standards. The Starbase Graphics Library provides high performance graphics based on the evolving Computer Graphics Interface standard from ANSI. HP GKS implements the Graphics Kernel System standard from ANSI and ISO. X-Window supports construction of window-based user interfaces across networked systems and is based on a multi-vendor de facto standard. Display List supports hierarchical display lists for modeling of graphics data. For migration of existing HP 1000 and HP 9000 applications based on DGL and AGP, a DGL/AGP Library package is provided.

Some models of the Series 800 also provide advanced bit-mapped graphics capabilities when configured with their respective Solid Rendering Display Subsystems. These models implement state-of-the art graphics algorithms in hardware and firmware to provide high speed performance for high end graphics applications.

Program Languages

HP-UX supports a rich development environment, including the HP Assembler, C Compiler, Profiler, Path Flow Analysis tools, and a screen oriented Symbolic Debugger. Several levels of optimization are supported to maximize object code efficiency. Additional packages offered include compilers for FORTRAN 77 and Pascal with optimization and full symbolic debug support.

Device I/O Library

A Device I/O Library (DIL) simplifies programming for controlling and communicating with peripheral devices and instruments connected to a Series 800 system via the HP 27110B HP-IB interface or the HP 27114A Parallel AFI interface.

System Networking

The Series 800 connects to HP 9000, HP 1000 A-Series, across HP product lines, and other vendors equipment via HP's networking products. These networking services are provided over the high speed IEEE 802.3 Standard Local Area Network (LAN) Link. The hardware and software interface, plus the transport facility are provided over the HP LAN/9000 Series 800 Link product. Higher-level Network Services are supported by the NS/9000 Series 800 software and the ARPA/BSD Series 800 product. Together, these software products support Remote File Access (RFA) between the HP-UX based HP 9000 systems, Network File transfer (NFT) with HP 9000 and HP 1000 systems, Network Interprocess Communication (NET IPC) within the HP 9000 Series 800 computer family, and virtual terminal capabilities. For more specific information on software availability for a particular Series 800 system, please refer to the HP 9000 Series 800 Computer System's Pricing Book, HP Literature Stock Number 5954-7055.

In addition to LAN communication, the Series 800 systems can communicate with other UNIX systems via one or more multiplexor channels and hardwired modem links using the UUCP capability of the HP-UX operating system. The UUCP capabilities include file transfer, remote command execution (UUX), and terminal emulation (CU). HP-UX electronic mail uses the UUCP facility.

ARPA/Berkeley networking services based on TCP/IP protocol are also available for the Series 800 systems.

Database Management

Database management is provided by the uniquely versatile ALLBASE/ HP-UX Database Management System (DBMS). The ALLBASE DBMS features both a relational data model HPSQL interface and a network model HPIMAGE interface for upward compatibility with existing IMAGE/1000 databases. Also, available is HP VISOR, a menu driven query and report package.

HPtoday

The HPtoday Developer Pack is a software system for computer-assisted development of applications. HPtoday applications are developed by filling in blanks on formatted screens instead of coding reams of program instructions. By bridging the gap between conception and the resulting application, HPtoday significantly shortens the time required to develop useful, bug-free applications, which will greatly improve software productivity. The HPtoday Run-Time Environment supports execution of developed HPtoday applications on target systems.

HP 1000 Applications Migration

The Series 800 systems include PORT/HP-UX package to help customers move applications from HP 1000 systems operating under the RTE-A or RTE-6/VM environment to the HP-UX environment. In addition to emulation of most RTE calls on HP-UX, PORT/HP-UX provides tools for analyses of applications to determine what program statements need to be modified as well as providing instructions on the type of modification.

Futhermore, PORT/HP-UX and the new ALLBASE/HP-UX DBMS provide facilities for migration of IMAGE/1000 and IMAGE/1000-II databases. The DGL and AGP libraries for the Series 800 systems have only slight differences from the DGL and AGP libraries on the HP 1000 systems, thus simplifying migration of graphics applications to the HP 9000 Series 800 systems. For more information on HP 1000 migration, refer to the HP 9000 Series 800 Software Technical Data book, HP Literature Stock Number 5953-8788.

HP 9000 Applications Migration

Applications currently running under HP-UX on HP 9000 Series 200, 300, or 500 computer systems are highly code compatible with the Series 800 systems. In many cases, all that is required to port a current application to the Series 800 systems is a simple recompilation of the code. For the Series 800 family, most applications are object code compatible.

HP 9000 Model 825S/SRX

The Model 825S/SRX are the entry level members of the Series 800 family. They run on HP-UX and utilize HP's proprietary VLSI NMOS III technology. Offering the best performance in their price class, the Model 825S/SRX feature the unique combination of low price, high computational performance, high speed bit mapped graphics, and HP-UX.

Functional Specifications

Capacity

Memory:

Model 825S: 8MB ECC, expandable to 56MB.

Model 825SRX: Expandable to 48MB.

Battery Backup: Sustains 56 MB of memory for at least 15 minutes when fully charged.

Available I/O Slots:

Model 825S: 7 slots minimum, of which two are used by the multiplexor and HP-IB interface card that are included in the basic Model 825S system.

Model 825SRX: 7 CIO slots minimum, of which three are used by the HP-IB, LAN, and Display Controller interfaces that are included in the basic Model 825SRX system.

Terminals:

Model 825S: 30 terminals max without I/O expander, 64* terminals max with A1013A I/O expander.

Workstations:

Model 825SRX: 4 Solid Rendering Display subsystems supported.

Disc Memory: The HP-IB interface furnished with the Model 825S/SRX system can connect up to four separate disc drives to the system. Supported disc drives range from 132MB to 571MB capacities. The total number of disc drives which can be connected is 12 for a maximum of 6.85GB of memory.

Central Processor Unit

Word Size: 32 bits.

Physical Address Space: 28 bit address (256 MB).

Virtual Memory Address Space: 48 bit address (281,000 GB).

Base Instruction Set: 135 instructions.

Base Instruction Cycle Time: 80 ns.

Translation Lookaside Buffer: 2048 entries.

Estimated Relative Throughput: 0.5 to 0.7 (840S = 1.0)

*This is the current maximum tested number of concurrent users. The physical maximums are 72 RS-232C devices for the Model 825S with I/O expanders.

**Supported as System Console with option S12.

†NOTE 7936H/7937H is highly recommended as system disc because of its high capacity.

Floating Point Capability

Floating Point Instructions: 40 instructions.

Floating Point Speed: 2.4 million double precision WHETSTONES per second.

Floating Point Format: ANSI/IEEE 754-1985 standard.
Input/Output I/O Addresses: Determined programmatically and by card slot location.

Direct Memory Access: Data chaining and command chaining are supported with 32-bit count and address.

DMA Bandwidth: 4.8 MB/sec for transfers via the 27114A Parallel Async FIFO Interface. 3.1MB/sec total bandwidth available per Channel I/O Adapter for transfers via the 27110B HP-IB Interface, the 27140A Six-Channel Multiplexor, or the LAN/9000 interface.

Data Packing: DMA transfers must be aligned to 32-byte boundaries in memory.

Supported Peripherals

Supported Terminals

HP 2392A Display Terminal**
HP 2393A Graphics Terminal
HP 2394A Data Entry Terminal
HP 2397A Color Graphics Terminal with 35741A Monitor
HP 45711A Portable Plus Computer
HP 45610B Touchscreen Terminal
HP 45850A Touchscreen II Terminal
HP 45851A Touchscreen II Personal Computer
HP 72425A VECTRA PC (req. 35731A or 35741A)
HP 72435A VECTRA PC (req. 35731A or 35741A)
HP 72445A VECTRA PC (req. 35731A or 35741A)
HP 9807A INTEGRAL Personal Computer
HP 98561A Model 310 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)
HP 98561B Model 320 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)
HP 98562A Model 330 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)
HP 98562B Model 350 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)

Supported Discs

HP 7933H 404 MB CS/80 Fixed Disc
HP 7935H 404 MB Removable Media CS/80 Disc
HP 7936H† 307 MB CS/80 Fixed Disc
HP 7937H† 571 MB CS/80 Fixed Disc
HP 7914CT 132.1 MB CS/80 Fixed Disc w/CTU backup
HP 7914P/R 132.1 MB CS/80 Fixed Disc w/CTU backup
HP 7914ST 132.1 MB CS/80 Fixed Disc and 1600 cpi Mag Tape Unit, cabinet included

Supported Magnetic Tape Units

HP 7974A Magnetic Tape Unit
HP 7978B Magnetic Tape Unit
HP 35401A Cartridge Autochanger Tape Subsystem
HP 9144A CS/80 Cartridge Tape Subsystem

Supported Printers

HP 2563B 300 LPM Dot Matrix Line Printer
HP 2564B 600 LPM Dot Matrix Line Printer
HP 2566B 900 LPM Dot Matrix Line Printer
HP 2567B 1200 LPM Dot Matrix Line Printer
HP 2686A + 300 LaserJet Plus Printer
HP 2684A LaserJet 2000 RS-232C Printer
HP 33440A LaserJet Series II Printer
HP 2934A 200/67/40 cps Office Printer
HP 2932A 200 cps Office Printer
HP 2225D ThinkJet RS-232C Printer
HP 2227A QuietJet RS-232C Printer
HP 2228A QuietJet Plus RS-232C Printer

Supported Plotters

HP 7440A 8-pen ColorPro Plotter
HP 7475A 6-pen Plotter
HP 7550A 8-pen Plotter w/auto sheet feed
HP 7586B 8-pen Roll-Feed Drafting Plotter
HP 7595A 8-pen DraftMaster I Plotter
HP 7596A 8-pen DraftMaster II Plotter

Supported Data Communications Devices

HP 37212 Intelligent 300/1200 baud modem
HP 92205A Hayes Smartmodem 1200™
HP 92223A LAN Repeater Kit

NOTE: For other LAN connection accessories, see the Hewlett-Packard Computer User's Catalog.

Electrical Specifications

AC Power Input

Voltage/Frequency:

Range 1: 90 to 127 VAC, 47.5 to 66Hz.
77 to 143 VAC, 45.0 to 66Hz.
Range 2: 180 to 254 VAC, 47.5 to 66Hz.
154 to 286 VAC, 45.0 to 66Hz.

Maximum Power Required: 600 W.

Maximum Operating Current: 9.5 A

DC Current Available and Required for I/O Interfaces and Accessories The Model 825S/SRX system power supply provides enough current and power for any combination of I/O interfaces or other plug-in cards that can be installed in the system's card cage.

SPU Environmental Specifications

Temperature

Operating: 0° to 55° C (32° to 131°F).

Non-operating: -40° to 75° C (-40° to 167°F).

Altitude: Operating: up to 4.6 km (15,000 ft.).

Non-operating: up to 15.3 km (50,000 ft.).

Relative Humidity: 15 to 95 percent, at 0° to 47° C non-condensing.

Vibration and Shock

The HP 9000 Model 825S/SRX Systems are type tested for normal shipping and handling shock and vibration (contact factory for review of any application that requires operation under continuous vibration).

Acoustics

50 dB (A) Sound Power up 30°C.

Regulatory Compliance

Safety

UL Listed CSA Certified IEC 380/435 compliant

Electromagnetic Interference

Complies with FCC Class A. Manufacturers declaration verifies VDE level B.

Physical Characteristics

Dimensions

Height: 234 mm. (9.21 in.)

Width: 325 mm. (12.8 in.)

Depth: 500 mm. (19.7 in.)

Weight

23 kg (51 lbs.).

Ventilation

Forced air cooling where air flows from front to back.

Ordering Information

NOTE: HP A1004A SPU's require a terminal and a disc (not included) for operator communication and for the operating system and program development support. A magnetic tape unit is strongly recommended for software installation and backup and is required when an HP 793XH is the system disc.

HP A1004A System Processor Unit for the HP 9000 Model 825S System

The HP A1004A System Processor Unit includes:

1. Processor with 8 MB ECC memory, floating point coprocessor, six-channel multiplexor and HP-IB disc interfaces, 5 available I/O slots, 6 available memory slots, and SPU package.
2. HP-UX Version A.B1, 16 user, featuring C compiler and the HP-UX Symbolic Debugger. Also includes Assembler, Device I/O Library, Real-Time package, and PORT/HP-UX. On-line diagnostics and manuals listed in the HP-UX data sheet in the HP 9000 Series 800 Software Technical Data book are provided. Must order software Media Option AA0 or AA1.
3. Hardware and Software Documentation.
4. Site Preparation Consultation.

5. On-site installation assistance and checkout by a Hewlett-Packard Service Engineer, including integration and test with primary system.
6. 90-day on-site warranty.

HP A1005A System Processor Unit for the HP 9000 Model 825SRX System

The HP A1005A System Processor Unit includes:

1. Processor with 8 MB ECC memory, floating point coprocessor, HP-IB disc interface, LAN/9000 Series 825 Link, Display Controller interface, 4 available I/O slots, 5 available memory slots, and SPU package.
2. HP-UX Version A.B1, 16 user, featuring C compiler and the HP-UX Symbolic Debugger. Also includes Assembler, Device I/O Library, Real-Time package, PORT/HP-UX, X-Window, and ARPA. On-line diagnostics and manuals listed in the HP-UX data sheet in the HP 9000 Series 800 Software Technical Data book are provided. Must order software Media Option AA0 or AA1.
3. Solid Rendering Display Subsystem which includes 8 plane frame buffer, HP-HIL two button mouse, ITF keyboard, buffer box, ID module, 3D solid graphics accelerator, solid rendering display controller with 4 plane memory overlay, RGB cables, and 19" high resolution color monitor.
4. Hardware and Software Documentation.
5. Site Preparation Consultation.
6. On-site installation assistance and checkout by a Hewlett-Packard Service Engineer, including integration and test with primary system.
7. 90-day on-site warranty.

Hardware Options

AA0: Software on CS/80 cartridge tape.

AA1: Software on 1600 cpi mag tape.

Additional Memory, I/O Cards, and Terminal Cable Management Accessories

A1009A 2 MB ECC Memory Card

A1010A 8 MB ECC Memory Card

27110B HP-IB Interface with 27110B Option 800 (cable length = 2 metre).

27140A 6-Channel Multiplexor with 27140A Option 800 interface-to-connector panel cable (cable length = 4 metre).

27114A Parallel Asynchronous FIFO Interface Card (see 27114A data sheet to determine appropriate options for ordering).

91786A LAN/9000 Model 825 Link for communication over IEEE 802.3 compatible LAN. Link software is supplied on CS/80 cartridge tape unless Media Option AA1 is ordered to request software on 1600 cpi mag tape. The HP 91786A product is orderable only with the NS/9000 Series 825 product, listed below.

91787A/R NS/9000 Model 825 Network Services Software for Network File Transfer and Remote File Access. Orderable only with the 91786A LAN/9000 Model 825 product. Software is on CS/80 cartridge unless Media Option AA1 is ordered to request software on 1600 cpi mag tape.

50981A/ARPA/BSD Model 825 Networking Software.

Orderable only with the HP 91786A LAN/9000 Series 825 Link product. Software is on CS/80 cartridge unless Media Option AA1 is ordered to request the software on 1600 cpi mag tape.

A1013A I/O Expander. Includes power supply, card cage, package, channel adapter card, buffer card, and cable. Adds 7 CIO slots.

A1014A Battery Backup System. Includes batteries, charger, and cable.

A1015A Access Port Kit. Includes AP card, connector panel, and cable. Requires one port of an existing 6-channel multiplexor card.

97099A 19" Rack Mount Kit for Model 825S/SRX SPU.

19500B 19" Rack Mount Kit for Model 825S/SRX Battery Backup Unit.

98720A Solid Rendering Display System with 4 plane memory overlay.

98721A 3D Solid Graphics Accelerator.

A1017A Display Controller Interface.

98723A Additional Power Supply for 16, 24, or 32 planes for the Model 825/SRX.

98722A 8 Plane Frame Buffer Memory for 825SRX.

46021A ITF Keyboard.

46060A HP-HIL 2-button mouse.

46081A Buffer Box with Speaker.

46084A ID Module.

98784A 19" Color Monitor (1280 x 1024).

Upgrading HP-UX Licenses

92453A HP-UX 32-user license with same software as listed in A1004A, item 2, above. Must order software Media Option AA0 or AA1, listed above.

-0A0 Credit upgrade to upgrade from 16-user license.

92454A HP-UX 64-user license with the same software as listed in A1004A, item 2, above. Must order software Media Option AA0 or AA1, listed above.

-0A1 Credit for upgrade from 16-user license.

-0A2 Credit for upgrade from 32-user license.

HP 9000 Model 850S

The Model 850S is the fastest member of the Series 800 family. It runs HP-UX and utilizes HP's proprietary VLSI NMOS III technology. Offering higher performance and more expandability than the Model 825S/SRX and 840S, the 850S represents a high capacity, high performance extension to both the HP 9000 and the HP 1000 product lines.

Functional Specifications

Capacity

Memory: 16 MB ECC memory, expandable to 128 MB.

Battery Backup: Sustains 128 MB of memory for at least 15 minutes when fully charged.

Available I/O Slots: 10 CIO slots minimum, of which three are used by the multiplexor, HP-IB interface card, and the Access Port card which are included in the basic Model 850S SPU. (20 CIO slots maximum supported at first release).

Terminals: The multiplexor card furnished with the Model 850S SPU can connect the system console, a modem for remote support, and four other terminals or other RS-232C devices to the system. With additional multiplexors with their corresponding channel adapters, up to 90 terminals can be supported at first release.

Disc Memory: The HP-IB interface furnished with the Model 850S SPU can connect up to four separate disc drives to the system. Supported disc drives range from 132MB to 571MB capacities. Additional interfaces can each connect more discs to the system.

Central Processor Unit

Word Size: 32 bits.

Physical Address Space: 29 bit address (512 MB).

Virtual Memory Address Space: 48 bit address (281,000 GB).

Base Instruction Set: 135 instructions.

Base Instruction Cycle Time: 73 ns.

Translation Lookaside Buffer: 4096 entries.

Estimated Relative Throughput: 1.5 to 1.6 (840S = 1.0)

Floating Point Capability

Floating Point Instructions: 40 instructions.

Floating Point Speed: 2.9 million double precision WHETSTONES per second.

Floating Point Format: ANSI/IEEE 754-1985 standard.

Input/Output

I/O Addresses: Determined programmatically and by card slot location.

Direct Memory Access: Data chaining and command chaining are supported with 32-bit count and address.

DMA Bandwidth: 4.8 MB/sec for transfers via the 27114A Parallel Async FIFO Interface. 3.1MB/sec total bandwidth available per Channel I/O Adapter for transfers via the 27110B HP-IB Interface, the 27140A Six-Channel Multiplexor, or the LAN/9000 interface.

Data Packing: DMA transfers must be aligned to 32-byte boundaries in memory.

Supported Peripherals

Supported Terminals

HP 2392A Display Terminal**
HP 2393A Graphics Terminal
HP 2394A Data Entry Terminal
HP 2397A Color Graphics Terminal with 35741A Monitor
HP 45711A Portable Plus Computer
HP 45610B Touchscreen Terminal
HP 45850A Touchscreen II Terminal
HP 45851A Touchscreen II Personal Computer
HP 72425A VECTRA PC (req. 35731A or 35741A)
HP 72435A VECTRA PC (req. 35731A or 35741A)
HP 72445A VECTRA PC (req. 35731A or 35741A)
HP 9807A INTEGRAL Personal Computer
HP 98561A Model 310 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)
HP 98561B Model 320 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)
HP 98562A Model 330 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)
HP 98562B Model 350 System Processor Unit (req. 35731A, 35741A, 98791A, or 98782A monitor)

Supported Discs

HP 7933H 404 MB CS/80 Fixed Disc
HP 7935H 404 MB Removable Media CS/80 Disc
HP 7936H* 307 MB CS/80 Fixed Disc
HP 7937H* 571 MB CS/80 Fixed Disc
HP 7957A 81 MB CS/80 Fixed Disc
HP 7958A 130 MB CS/80 Fixed Disc
HP 7914CT 132.1 MB CS/80 Fixed Disc w/CTU backup
HP 7914P/R 132.1 MB CS/80 Fixed Disc w/CTU backup
HP 7914ST 132.1 MB CS/80 Fixed Disc and 1600 cpi Mag Tape Unit, cabinet included.

*NOTE 7936H/7937H is highly recommended as system disc because of its high capacity.

**Supported as System Console with option S12.

Supported Magnetic Tape Units

HP 7974A Magnetic Tape Unit
HP 7978B Magnetic Tape Unit
HP 35401A Cartridge Autochanger Tape Subsystem
HP 9144A CS/80 Cartridge Tape Subsystem

Supported Printers

HP 2563B 300 LPM Dot Matrix Line Printer
HP 2564B 600 LPM Dot Matrix Line Printer
HP 2566B 900 LPM Dot Matrix Line Printer
HP 2567B 1200 LPM Dot Matrix Line Printer
HP 2686A + 300 LaserJet Plus Printer
HP 2684A LaserJet 2000 RS-232C Printer
HP 33440A LaserJet Series II Printer
HP 2934A 200/67/40 cps Office Printer
HP 2932A 200 cps Office Printer
HP 2225D ThinkJet RS-232C Printer
HP 2227A QuietJet RS-232C Printer
HP 2228A QuietJet Plus RS-232C Printer

Supported Plotters

HP 7440A 8-pen ColorPro Plotter
HP 7475A 6-pen Plotter
HP 7550A 8-pen Plotter w/auto sheet feed
HP 7586B 8-pen Roll-Feed Drafting Plotter
HP 7595A 8-pen DraftMaster I Plotter
HP 7596A 8-pen DraftMaster II Plotter

Supported Data Communications Devices

HP 37212 Intelligent 300/1200 baud modem
HP 92205A Hayes Smartmodem 1200™
HP 92223A LAN Repeater Kit

NOTE: For other LAN connection accessories, see the Hewlett-Packard Computer User's Catalog.

Electrical Specifications

AC Power Input

Voltage/Frequency:

208 VAC (+/- %10), 3 phase @ 60Hz (+/- %2)
380 VAC (+/- %10), 3 phase @ 50Hz (+/- %2)
408 VAC (+/- %10), 3 phase @ 50Hz (+/- %2)

Maximum Power Required: 3500 W.

Maximum Operating Current:

16A @ 208 VAC
8.0A @ 380 VAC
7.5A @ 415 VAC

DC Current Available and Required for I/O Interfaces and Accessories The Model 850S system power supply provides enough current and power for any combination of I/O interfaces or other plug-in cards that can be installed in the system's card cage.

SPU Environmental Specifications

Temperature

Operating: 5° to 40° C (41° to 104° F).

Non-operating: -40° to 70° C (-40 to 158°F).

Altitude: Operating: up to 4.6 km (15,000 ft.).

Non-operating: up to 15.3 km (50,000 ft.).

Relative Humidity: 20 to 80 percent, at 40° C non-condensing.

Vibration and Shock

The HP 9000 Model 850S Systems are type tested for normal shipping and handling shock and vibration (contact factory for review of any application that requires operation under continuous vibration).

Acoustics

73 dB (A) Sound Power.

Regulatory Compliance

Safety

UL Listed CSA Certified IEC 380/435 compliant

Electromagnetic Interference

Complies with FCC Class A, and FTZ Individual Permit (Level A Serial License).

Physical Characteristics

Dimensions

Height: 1000 mm. (39.4 in.)
Width: 1300 mm. (51.2 in.)
Depth: 710 mm. (27.9 in.)

Weight

400 kg (880 lbs.).

Ventilation

Forced air cooling where air flows from top to bottom.

Ordering Information

NOTE: HP 9742A SPU's require a terminal and a disc (not included) for operator communication and for the operating system and program development support. A magnetic tape unit is strongly recommended for software installation and backup and is required when an HP 793XH is the system disc.

HP 9742A System Processor Unit for the HP 9000 Model 850S System

The HP 9742A System Processor Unit includes:

1. Processor with 16 MB ECC memory, floating point coprocessor, six-channel multiplexor and HP-IB disc interfaces, access port card, 7 available I/O slots, and power distribution unit with power cable in a 1-metre cabinet.
2. HP-UX Version A.B1, 32 user, featuring C compiler and the HP-UX Symbolic Debugger. Also includes Assembler, Device I/O Library, Real-Time package, and PORT/HP-UX. On-line diagnostics and manuals listed in the HP-UX data sheet in the HP 9000 Series 800 Software Technical Data book are provided. Must order software Media Option AA0 or AA1.
3. Hardware and Software Documentation.
4. Site Preparation Consultation.
5. On-site installation assistance and checkout by a Hewlett-Packard Service Engineer, including integration and test with primary system.
6. 90-day on-site warranty.

Hardware Options

516: Additional 16MB Main Memory.

AA0: Software on CS/80 cartridge tape.

AA1: Software on 1600 cpi mag tape.

015: 380 VAC, 50Hz.

016: 415 VAC, 50Hz.



Software Options

0B0: Delete manuals.

0C8: Upgrade from Model 825S/SRX to Model 850S.

0C9: Upgrade from Model 840S to Model 850S.

0CC: Upgrade without current support.

Additional Memory, I/O Cards, and Terminal Cable Management Accessories

A1104A 16 MB ECC Memory Card

A1101A CIO Channel Adapter

27110B HP-IB Interface with 27110B Option 800 (cable length = 2 metre).

27140A 6-Channel Multiplexor with 27140A Option 800 interface-to-connector panel cable (cable length = 4 metre).

27114A Parallel Asynchronous FIFO Interface Card (see 27114A data sheet to determine appropriate options for ordering).

91788A LAN/9000 Model 850S Link for communication over IEEE 802.3 compatible LAN. Link software is supplied on CS/80 cartridge tape unless Media Option AA1 is ordered to request software on 1600 cpi mag tape. The HP 98788A product is orderable only with the NS/9000 Model 850S product, listed below.

91789A/R NS/9000 Model 850S Link Network Services Software for Network File Transfer and Remote File Access. Orderable only with the 91788A LAN/9000 Series 850 product. Software is on CS/80 cartridge unless Media Option AA1 is ordered to request software on 1600 cpi mag tape.

50982A/R ARPA/BSD Model 850S Networking Software. Orderable only with the HP 91788A LAN/9000 Series 850 Link product. Software is on CS/80 cartridge unless Media Option AA1 is ordered to request the software on 1600 cpi mag tape.

19749A Cable Management System for housing up to 11 multiplexer connector panels and managing the associated interconnect cables. The connector panel compartment is mounted on the rear of a system console support table.

Upgrading HP-UX Licenses

92454A HP-UX 64-user license with same software as listed in 9742A, item 2. Must order software Media Option AA0 or AA1.

-0A2 Credit upgrade from 32-user license.

92455A HP-UX Unlimited license with same software as listed in 9742A, item 2. Must order software Media Option AA0 or AA1.

-0A2 Credit upgrade from 32-user license.

-0A3 Credit upgrade from 64-user license.

Additional Software

(Must order software media option AA0 or AA1)

92461A/R FORTRAN 77/HP-UX compiler for the Model 850S.

92462A/R Pascal/HP-UX compiler for the Model 850S.

92463A/R Starbase/HP-UX graphics library for the Model 850S.

92464A/R DGL/AGP/HP-UX graphics libraries for the Model 850S.

92465A/R Development Pack (includes: FORTRAN 77 and Pascal compilers, DGL/AGP and Starbase graphics libraries) for the Model 850S.

35307 HPtoday Developer Pack (includes HPtoday Run Time Environment) for the Model 850S.

35308A HPtoday Run Time Environment for the Model 850S.

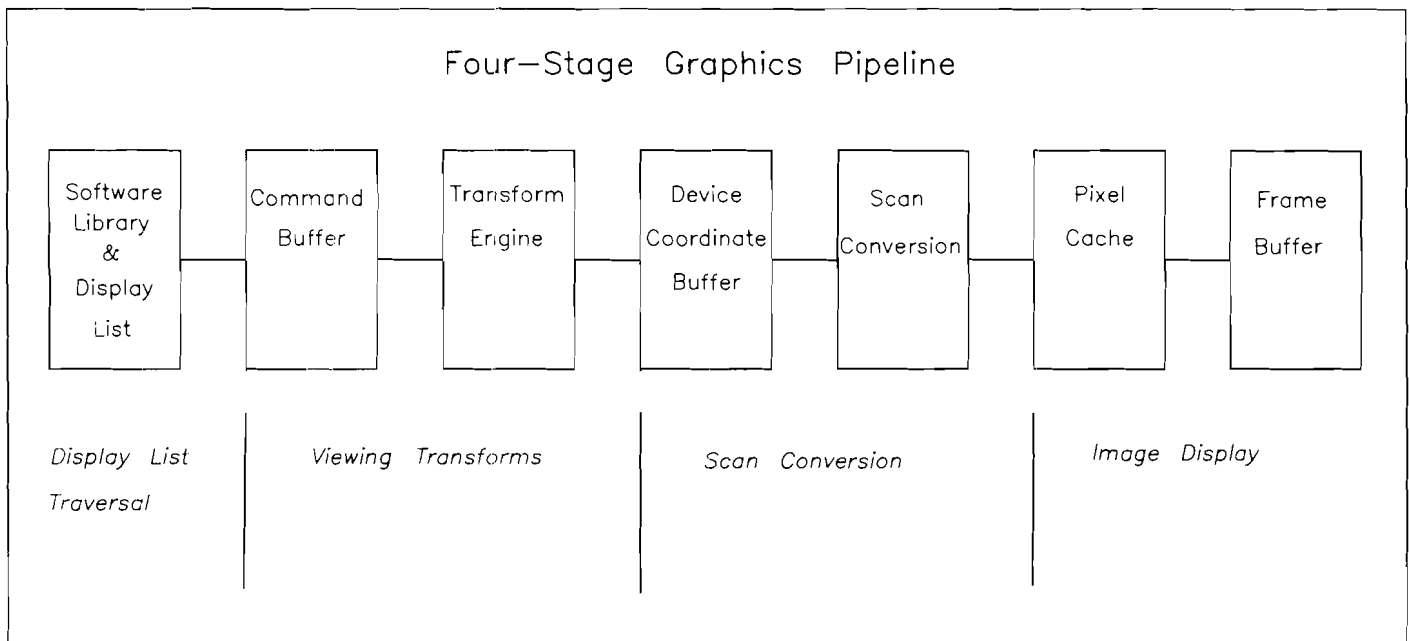
92468A ALLBASE and HPtoday Developer Pack bundle for the Model 850S.

92469A/R ALLBASE/HP-UX Relational and IMAGE database management system package with IMAGE/1000 translator for the Model 850S.

92535A/R HP VISOR user friendly interface to HP SQL for the Model 850S.

92529A/R HP GKS Graphics Kernal Standard graphics package for the Model 850S.





Note: The transform engine and scan converter make up the graphics accelerator.

Graphics Architecture and Performance

The architecture of the SRX is based upon a traditional four-stage graphics pipeline. But most four-stage graphics pipeline systems on the market today have performance bottlenecks in the pipeline. Although one part of the pipeline can be very fast, others are typically very slow. This causes the overall system performance to be slow. And because of this, graphics vendors tend to specify only the faster portions of their pipeline such as *transforms per second*.

To obtain interactive graphics performance, the traditional graphics pipeline has been modified:

- Dual-ported memory has been added between each stage of the graphics pipeline, allowing each stage to operate independently, increasing the throughput of the pipeline
- VLSI was used to eliminate pipeline bottlenecks

Solid rendering requires specialized features. Key features such as light sources, shading, hidden-surface removal and B-splines have been implemented in hardware and micro-code. HP's B-spline implementation allows you to generate curved lines, meshes, and surfaces from control points and knot vectors. Automatic light sources, shading, and hidden-surface removal give the B-spline surface the same

definition as that found in a surface defined by polygons. However, the amount of data required to generate the surface is greatly reduced and performance is vastly improved.

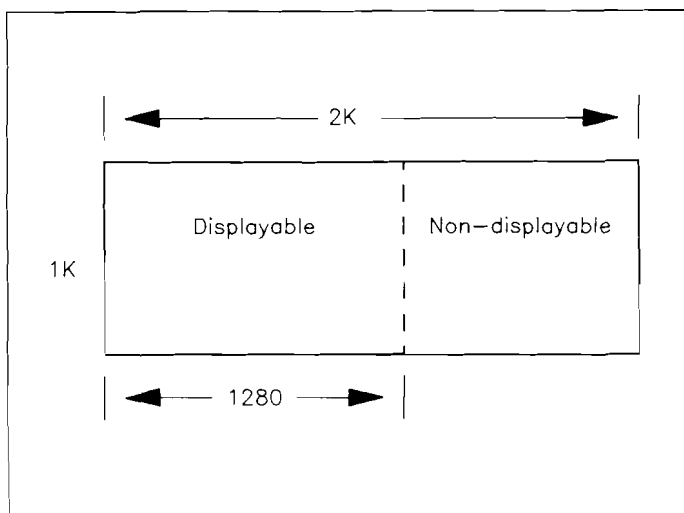
Graphics Hardware

Display Controller (HP 98720A)

The Display Controller provides the resolution and number of displayable colors necessary for high-end graphics applications such as solid rendering, image processing, Architecture and Engineering Construction (AEC) and petroleum exploration. It offers four frame buffer planes at the entry level.

Overlay planes provide the capability to do windowing, cursors, menus and alpha independently of the frame buffer. The availability of four overlay planes allows these capabilities to be done in multiple colors. Frame buffer memory (Option 722 or HP 98722A upgrade) can be added in increments of eight planes, for a total of 32 planes frame buffer memory and four overlay planes. A 32 plane system offers 16.7 million simultaneously displayable colors with a 24-plane frame buffer and 8 planes dedicated to full 16-bit Z-buffer.*

*The 16-bit full Z-buffer is available when a graphics accelerator is installed.



The Display Controller supports 1280 x 1024 displayable pixels. However, 2 Kbyte x 1 Kbyte Video RAM is required, the non-displayable portions being used for Z-buffering (see above).*

Graphics Accelerator (HP 98720A Option 721 or HP 98721A Upgrade)

The Graphics Accelerator contains a bit-slice processor with writable control store and floating point integrated circuits for add, multiply and divide functions. This provides the hardware and microcode implementation of the routines required by 3-D applications, routines such as:

- Light source
- Shading
- Hidden-surface removal
- B-splines

Hidden-surface removal requires frame buffer memory (HP 98720A Option 722 or HP 98722A Upgrade). The non-displayable portion of the frame buffer can be used if a low-cost strip-Z-buffer system is needed. However, adding an extra frame buffer board to the system allows hidden-surface removal performance to increase by three times using full 16-bit Z-buffer.

19-inch High-resolution Color Monitor (HP 98784A)

The HP 98784A is a 1280 x 1024 resolution, 19-inch color monitor. This high-quality monitor has a 60-Hz non-interlaced refresh rate, and a P22 phosphor for "true-to-life" colors. The CRT offers a clear, vivid image that doesn't wash out. The cylindrical face and antiglare coating are ergonomic design features for maximum eye comfort.

Cabling Extensions/Input Devices (HP-HIL, Audio, RGB)

Through HP cabling extensions, human interface devices such as the display, keyboard, mouse and control dials can be placed up to 30 meters from the host SPU and graphics subsystem. Cabling is provided for three types of signals.

- HP-HIL for the keyboard, mouse and other HP-HIL input devices
- Audio for the speaker (included with each cabling extension) to provide audio output for the system
- RGB for the video signals to the color display

The extensions are compatible with the standard HP-HIL interface and RS-343 video requirements. No power cords are required as cabling power comes from the host system. For more information and the specifications of these devices please refer to the HP-HIL Devices Technical Data Sheet (Publication Number 5953-9584).

Technical Specifications† Display Controller (HP 98720A)

Frame buffer size:

2048 x 1024

Frame buffer planes:

4, 8, 16, 24, or 32 (maximum 24 displayable, additional 8 planes and non-displayable portions of Video RAM provide full 16-bit Z-buffering).

Overlay planes:

0 (4-plane system)
4 (8, 16, 24, or 32-plane system)

Video signals:

RS-343

Color palette:

16.7 million

Mathematical representation:

32-bit floating point

Z-buffer:

Hardware, 16-bit full or strip

Control memory:

Writeable control store

Double buffering:

4, 8 or 12 planes

*The 16-bit full Z-buffer is available when a graphics accelerator is installed.

†Specifications listed are for a full system including a Graphics Accelerator, 32-plane frame buffer memory and four overlay planes.

Color Monitor (HP 98784A)

Screen size:

48 cm (19 in.) diagonal

Viewing area:

343 x 274 cm (14.0 x 10.5 in.)

Phosphor:

P22

Refresh rate:

60 Hz non-interlaced

Display resolution:

1280 x 1024

Brightness:

27 FL

Character font:

15 x 10 pixels

System Capabilities

Primitives

- Vectors
- Polylines
- Circles
- Arcs
- Polygons
 - n-sided, concave, convex, crossing, doughnut, wireframe
- B-splines (non-uniform rational, with trimming)
 - curved lines, meshes, surfaces

Image Rendering

- Depth Cueing
- Hidden-Surface Removal
- Flat Shading
- Gouraud Shading
- Phong Lighting Model
 - specular and diffuse reflections
- Lights (up to 8 sources, color and intensity adjustable)
 - directional, ambient, positional, spotlight, colored
- Transparency
- Perspective Projection

Software

- Starbase
 - CG-VDI-based
- Optional Display List
 - 3-D Hierarchical PHIGS-based
 - System memory or virtual memory, giving nearly unlimited size
 - Hierarchical segments
 - Segment contents editable
 - Picking supported

Dimensional Capabilities

- Geometric transformations
 - Scale, rotate, translate, perspective
 - Concatination of transformations
 - Light source and perspective
- 32-bit IEEE floating point
- 2-D and 3-D coordinates
- 6-plane clipping

Price/Performance Optimization Features

- Hardware dithering
- Back-facing polygon cull
- Double buffering
- Strip-Z-buffer hidden-surface removal

Peak Performance

Display list traversal:

190,000 vectors per second

Graphics accelerator:

180,000 coordinates per second

Scan conversion:

16 million pixels per second

Raster operations:

125 million pixels per second using rectangle area fill

Area fill speed:

124 million pixels per second

Power Requirements*

	Display Controller and Accelerator (HP 98720A Opt. 721 or HP 98721A Upgrade)	Color Monitor (HP 98784A)
Line voltage (Vac)	90 - 125 or 198 - 250	90 - 125 or 198 - 250
Line frequency (Hz)	48 - 66	48 - 66
Current (A) requirements: @90 - 125 Vac @198 - 250 Vac	10.6 A maximum 6.5 A maximum	2.9 1.6
Power consumption (max): Main supply Auxiliary supply	370 Watts, 1262 BTU/hr 240 Watts, 818 BTU/hr	220 Watts, 750 BTU/hr

*Specifications listed are for a full system including a Graphics Accelerator, 32-plane frame buffer memory and four overlay planes.

Environmental Range

	Display Controller and Accelerator (HP 98720A Opt. 721 or HP 98721A Upgrade)	Color Monitor (HP 98784A)
Temperature: Operating Non-operating	0° - 55°C -40° - 75°C	10° - 40°C -40° - 60°C
Humidity: Operating 40°C	5% - 95%	10% - 80%
Altitude: Operating Non-operating	4,600 meters (15,000 ft.) 15,300 meters (50,000 ft.)	2,125 meters (7,000 ft.) 7,473 meters (25,000 ft.)
Electromagnetic interference (EMI): VDE level FCC class	A A	A A
Line transient immunity	1 Kv	1 Kv
Rise time	1 nsec	1 nsec
Width	800 nsec	800 nsec
Regulatory compliance	UL, CSA, IEC	UL, CSA, IEC, SEV, FEI

Physical Specifications

	Display Controller and Accelerator (HP 98720A Opt. 721 or HP 98721A Upgrade)	Color Monitor (HP 98784A)
Height	23.5 cm (9.3 in.)	44.9 cm (17.7 in.)
Width	32.5 cm (12.8 in.)	49.6 cm (19.5 in.)
Depth	55.0 cm (21.7 in.)	59.6 cm (23.5 in.)
Net weight	23.2 kg (51 lbs.)	40.7 kg (90 lbs.)

For HP 9000 Series 800 Systems

product number 27110B

The HP 27110B HP-IB* interface supports connection of up to 14 Hewlett-Packard Interface Bus (HP-IB) devices to HP 9000 Series 800 Systems. HP-IB devices include discs, printers, plotters, magnetic tape devices, graphics digitizers and an extensive list of instruments.

Features

- Simplified implementation of computer-controlled instrumentation and peripheral systems
- IEEE-488-1978 compatibility
- 980 kilobytes per second high speed, 500 kilobytes per second standard speed
- On-board intelligence that off-loads the host computer, freeing CPU resources for application processing
- Support of up to 14 standard devices or up to 8 high speed devices (standard speed devices are not usable on the high speed bus)
- Support of Command Set 80 protocol for CS/80-based discs and tapes
- Selectable HP-IB controller or slave capabilities
- Parity and Cyclic Redundancy Checks for error detection
- Programatic enabling/disabling of parallel polling
- Firmware-based self-test of interface integrity

HP-IB Capabilities

The 27110B HP-IB Interface connects to the signal lines shown in Figure 1, acting as DEVICE A. Eight bidirectional data bus lines carry coded messages in bit-parallel, byte-serial form to/from other devices on the bus, with each byte transferred from one "talker" to one or more "listeners". Data is exchanged asynchronously using interface messages to set up, maintain, and terminate an orderly flow of device-dependent messages. Three data byte transfer control lines control the transfer of each byte of coded data on the eight data lines. The five general interface management lines ensure an orderly flow of information within the HP-IB.

Functional Specifications

Capacity

High speed devices per 27110B interface: Up to eight with load resistors installed.

Standard speed HP-IB devices per interface: Up to 14.

NOTE: Standard speed devices cannot be mixed on a high speed bus. High speed devices can be mixed on a standard speed bus if high speed cabling rules are observed.

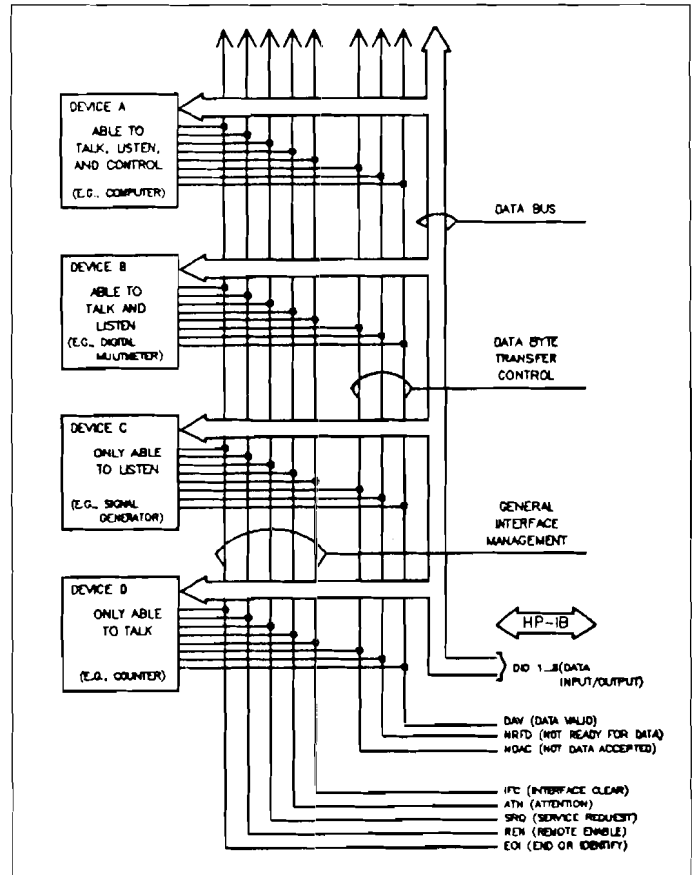


Figure 1. HP Interface Bus Concept

Operating Modes

High speed mode: Operation at data rates to 980 kilobytes per second.

Standard speed mode: Operation at data rates to 500 kilobytes per second.

NOTE: Realizable speed for a particular system is dependent on such factors as cable length, type of external devices, system level software and number of devices. Higher transfer rates can be achieved when using less than maximum cable lengths and devices. Consult system documentation for further information.

*The Hewlett-Packard Interface Bus (HP-IB) is HP's implementation of IEEE Standard 488-1978: "Digital interface for programmable instrumentation" and identical ANSI standard MC1.1. The term "HP-IB" is also used to identify Hewlett-Packard instruments conforming with this standard.

System controller mode: A two position switch enables or disables 27110B operation as system controller.

Bus Characteristics

HP-IB Bus Signal lines:

OIO1	Data Input/Output 1
OIO2	Data Input/Output 2
OIO3	Data Input/Output 3
OIO4	Data Input/Output 4
OIO5	Data Input/Output 5
OIO6	Data Input/Output 6
OIO7	Data Input/Output 7
OIO8	Data Input/Output 8
OAV	Data Valid
NRFD	Not Ready For Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Logic Levels: High > 2.4V/Low < 0.5V, all low-true

Supported HP-IB functions: C1-C5, SR1, RL2, PP1, DC1, SH1, AH1, T1, TE1, L1, LE1, DT1, E2. TE1 and LE1 require host system support.

Logic Levels, line terminations, line drivers, and line receivers: All characteristics conform to IEEE Standard 488-1978.

Maximum cable length for standard operation: 2 metres (6.5 ft) per device connected, with a 20 metre (65 ft) total length. The maximum number of devices is accommodated by interconnections using shorter than maximum cable length.

Maximum cable length for high speed operation: Interconnecting cable links should be as short as possible, with a maximum of 15 metres total length per system, and should have at least one equivalent resistive load per metre of cable (the high-speed resistor pack adds seven equivalent resistive loads).

Number of Devices	Maximum Total Cable Length (meters)
1	8
2	9
3	10
4	11
5	12
6	13
7	14
8 (maximum)	15

No more than eight devices are allowed in the system. A maximum system consists of the System Controller with its high-speed resistor pack and eight peripherals. Load resistors may need to be repositioned on the interface card for high speed operation. Refer to the installation manual.

NOTE: For high and low speed cable length operation, refer to the installation manual (27110-90005) for a complete explanation. The HP-IB connector mounting plate (30070-00043) should be used with extended cables. It is available from the Corporate Parts Center.

Error Detection

Data errors can be detected using Cyclic Redundancy Check-16 (CRC-16) on all data messages sent or received by another participating device that supports CRC-16. CRC-16 is invoked by the system for each transaction. See system documentation for details. Interface message errors are detected using odd byte parity.

Diagnostic Support

An interface resident self-test, initiated on reset, is provided in the firmware of the 27110B.

Direct Current Requirements

1.8A at +5V and 35 mA at +12V for total power dissipation of 9.42W.

Physical Characteristics

Dimensions: 172.7 mm (6.8 in.) long by 172 mm (6.75 in.) wide.

Weight: 234 grams (8.2 oz.); 679 grams (23.8 oz.) with HP-IB cable.

I/O Channel Interconnects: 80-pin connector, J1.

Device Interconnects: 26-pin connector, J2.

Environmental Specifications

Operating Temperature: 0° to 55°C (32° to 131°F).

Operating Humidity: 5% to 95% RH @ 40°C

Operating Altitude: 4600 metres (15,000 feet) maximum.

Ordering Information

HP 27110B HP-IB Interface

The 27110B includes:

27110-60201	HP-IB Interface Card
27110-63001	Two-metre HP-IB cable
27110-90005	Installation and Reference Manual
30070-00043	HP-IB Backing Plate

27110B Options:

0B0: Deletes the Installation and Reference Manual (27110-90005).

800: Deletes standard cable (27110-63001) and substitutes four metre female cable (27113-63001) for use with HP 9000 Series 800 Computers.

For HP 9000 Series 800 Systems

product number 27140A

The HP 27140A Multiplexer provides six asynchronous ports with full duplex modem control capability for connection of terminals or other RS-232-C devices to HP 9000 Series 800 Systems. A wide range of configurable transmission modes and formats supports direct or remote connection of CRT terminals, printers, plotters, and other asynchronous devices.

Features

- Six full-duplex asynchronous serial I/O ports with 10 wire modem control capability satisfying European license requirements.
- EIA RS-232-C and V.28 compatibility
- Full duplex modem operation only
- Supports local system console on port 0
- Programmable data rates for each channel
- Programmable character size: 5,6,7 or 8 data bits
- Programmable parity: odd, even, or none
- Programmable number of stop bits: 1, 1.5, or 2
- Parity, overrun, and framing error checks detect transmission faults
- Firmware based self-test of interface integrity
- Programmable device XON/XOFF handshaking to pace input and output data transmission
- On-board buffering with DMA capability to send/receive data to/from host for multiple ports in a single transfer

Functional Description

The HP 27140A Asynchronous 6-Channel multiplexer is used for interfacing up to six EIA RS-232-C compatible devices to the HP 9000 Series 800 System. As a Z80B microprocessor based interface, the HP 27140A MUX accesses a 16K byte EPROM which contains default port handling code for port zero and a power up self-test. Moreover, it monitors the download process and verifies the integrity of the code. The downloaded application software is optimized for character-at-a-time I/O.

Functional Specifications

Capacity

Channels: Six full-duplex channels

Buffering: On-card buffering with DMA capability to send/receive data for multiple ports in a single transfer increases throughput and reduces host CPU interrupts.

Transmit Buffer Size: 255 bytes per port.

Receive Buffer Size: Up to 1 Kbyte which is dynamically allocated among the 6 ports.

Communications

Interface Level: RS-232-C; CCITT V.28.

Data Rates: Baud rate defaults to 9600 and is software programmable to any of the following 15 rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19200.

Modem Support:

- originate mode
- auto answer mode
- modem connection timer
- lost receiver-ready timer
- no-activity timer
- host control of every interface output modem line

Supported Signal Lines:

RS-232-C	V.24	Common Abbrev.	Description	Input/Output
AB	102	SG	Signal Gnd	
BA	103	SD	Trans'd Data	O
BB	104	RD	Received Data	I
CA	105	RS	Req. to Send	O
CB	106	CS	Clear to Send	I
CC	107	DM	Dataset Ready	I
CD	108.2	TR	Data Ter Ready	O
CF	109	RR	Received Line Signal Detector	I
CH	111	SR	Sig. Rate Sel.	O
CE	126	IC	Ring Indicator	I

Throughput: The 27140A 6-channel MUX will support six interactive terminal users running character mode at 19.2K baud. Other RS-232-C applications which may simultaneously send and receive data over all six ports should be run at 9600 baud or slower.

Communication Mode: Asynchronous, bit serial.

Break Detection and Transmission: Break condition is recognized by the interface and causes an interrupt to be sent to the host. Break condition can also be generated by the interface at the request of the host.

Optional Device Handshakes: The MUX is capable of pacing both inbound and outbound data via an "XON/XOFF" type of protocol. The "XON/XOFF" characters are programmable. Outbound MUX transmission or device controlled "XON/XOFF" is performed at the interface level. Host controlled "XON/XOFF" is available to pace the flow of incoming data from a peripheral. This is not done at the interface level but on host demand.

Edit Functions

Edit functions such as backspace, character delete, and line delete are passed to the host and managed by the host operating system.

Direct Current Requirements

Voltage	Typical Current	Two Standard Deviation Current
+5V	1.380 A	2.298 A
+12V	0.084 A	0.159 A
-12V	0.135 A	0.150 A

Physical Characteristics

Dimensions: 172.7 mm (6.8 in.) long by 172 mm (6.75 in.) wide.

Weight: Interface Card 270 grams (9.5 oz.); Cable and RS-232 panel 723 gram (26 oz.).

Environmental Specifications

Operating Temperature: 0° to 55°C (32° to 131°F).

Operating Humidity: 5% to 95% RH @ 40°C.

Ordering Information

HP 27140A Asynchronous 6-Channel Multiplexer

The 27140A includes:

27140-60001	6-Channel Multiplexer Printed Circuit Assembly
28659-63002	1 meter interface to connector panel Cable
28659-60005	RS-232-C Connector Panel
27140-90006	Installation Manual

27140A Options

- 0B0:** Delete Manual (27140-90006).
- 001:** 10 meter Extension Cable (28659-63004) used with 28659-63002 to remotely position the RS-232-C connector panel.
- 019:** 19 inch Rack Mounting Bracket Kit (5061-4962).
- 800:** Deletes standard cable (28659-63002) and substitutes a longer 4 meter cable (28659-63006). Allows use with HP 9000 Series 800 computers.

A self-test hood connector for optional use with the on card self-test is available. Order HP Part Number 27140-60003.

Recommended Peripheral Cables

For direct connection to RS-232 terminals, printers, plotters, etc. minimum wiring requires pins 1, 2, 3, 7 to be wired end to end.

13242M	5 meter 25 pin M - 25 pin M pins 1-8, 12, 15, 17, 20, 22, 24 wired end to end
13242N	5 meter 25 pin M - 25 pin M pins 1-8, 12, 15, 17, 20, 22, 23, 24 wired end to end 11 and 19 are switched
13242Y	5 meter 25 pin M - 25 pin M 1-3, 7 wired end to end
92219G	3.8 meter 25 pin M - 25 pin M 1-8, 11, 12, 19, 20, 22, 23, 25 wired end to end

Connection to RS-232 Modems

92219Q 5 meter 25 pin M - 25 pin M

Computer End Pin Number	Data Set End Pin Number
1	1
2	3
3	2
4	8
6	20
7	7
8	4
9	22
20	6
22	5
23	23

For UUCP direct connect applications from 27140A to 27140A, the following cables could be used:

- 92219Q
- 30062B

The cables listed above are available from the Direct Marketing Division (DMK).

Recommended Modems

- HP 37212A Stand Alone Modem
- 92205A Hayes Smart Modem 1200
- Racal-Milgo MPS 1222 (Europe)
- US Robotics 2400 Baud
- Bell 212A



For HP 9000 Series 800 Systems

product number 27114A

The HP 27114A Parallel Asynchronous FIFO Interface is designed to provide multipurpose 8 or 16-bit parallel communication capabilities between external devices and HP 9000 Series 800 Systems.

Features

- 16-bit parallel interface
- Separate data input and output lines
- Differential or single-ended line drivers/receivers
- Configurable to GND true or +5V true
- Asynchronous handshaking mode (interlocked) only
- Half-duplex operation (only)
- Up to 66 words of FIFO buffering
- Three frontplane control lines
- Two frontplane status lines
- Two parity bits for software parity checking
- Host interrupt via Attention line
- Switch-selectable data settling time

Functional Specifications

Data Transfer

Protocol: Transfer either 8 or 16 parallel bits at a time, without byte packing on 8-bit transfers. The backplane channel can operate either in byte mode or word mode.

Maximum Transfer Rates: Actual transfer rate is system and block size dependent. With 3 metre differential cable:

Performance*	Block Size
3.9 Mbyte/s	> 64 bytes
4.7 Mbyte/s	< 64 bytes

Aggregate Transfer Rates: The aggregate throughput depends on the host processor, competing backplane activity and total transfer size. Throughput for 8 bit transfers will be roughly half that of the 16-bit transfers.

Maximum Distance: 50 meters

*The performance numbers shown above were measured on an HP 9000 Model 840. For more detailed information, please refer to AFI Performance Brief (P/N 5953-5029)

Backplane Polling

The 27114A is a group 0 polling device. This may impose certain backplane slot restrictions.

Line Characteristics

Signal Lines:

RD± 0-15	Received Data Positive/Negative Bus
SD± 0-15	Send Data Positive/Negative Bus
STS± 0-2	Status Input Positive/Negative Bus
CTL± 0-2	Control Output Positive/Negative Bus
RPAR± 0-1	Received Parity Positive/Negative Bus
SPAR± 0-1	Send Parity Positive/Negative Bus
PFLAG±	Peripheral Flag Positive/Negative
PCTL±	Peripheral Control Positive/Negative
ATTN±	Attention Positive/Negative
PDIR±	Peripheral Direction Positive/Negative
TEST-	Data Line Driver Enable (loopback hood detect)
GND 2	Signal Ground/Bus
SHIELD	Frame Ground

Logic Sense: Differential Mode — Logic sense is determined by the cable wiring. See example:

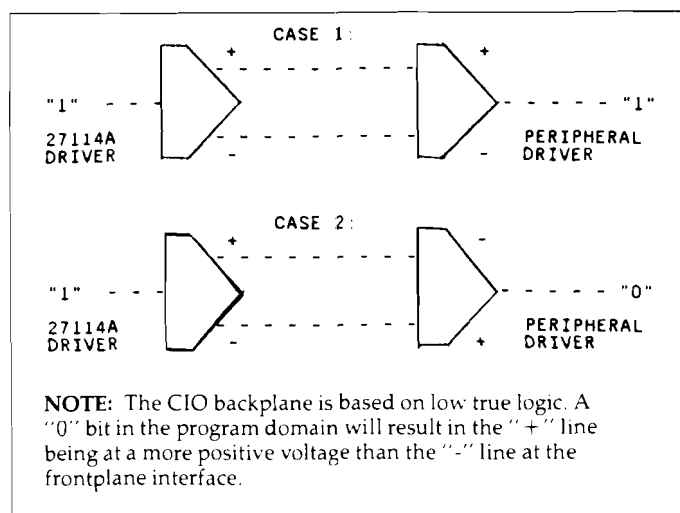


Figure 1

Single-ended Mode: Logic sense can be referenced to either +5V true or GND true. To minimize signal cross-talk, the optional single-ended cable should be used.

Internal Handshake Mode: The 27114A can also send data to or receive data from devices such as indicators or switches, that do not provide or use any type of handshake. This will require tying a control line to the peripheral flag line. Input data can be clocked on the rising or falling edge.

Control and Status Bit Communication

Control Output: Three control output bits may be sent to the interface device via an output control byte for use as control, command or address bits.

Status Input: Two status bits may be received from the interfaced device via an input control byte. The attention line can be programmed to cause an asynchronous request interrupt (ARQ).

Direct Current Requirements

Typically 2A at +5V; two standard deviation current is 2.25A.

Physical Characteristics

Dimensions: 172.2 mm (6.8 in.) long by 172 mm (6.75 in.) wide.

Weight: Interface Card, 243 grams (8.5 oz.); 3 meter cable 440 grams (15.5 oz.)

Environmental Specifications

Operating Temperature: 0° to 55°C (32° to 131°F).

Operating Humidity: 5% to 95% RH at 40°C.

Operating Altitude: 4600 metres (15,000 feet) maximum.

Comparison with Other HP Parallel Interfaces:

Features	27114A	27112A	12006	12566C	98622A
Backplane	CI/O	CI/O	AI/O	MEFI/O	DI/O
# of Data Bits	16 in/ 16 out	16 in/ 16 out	16 in/ 16 out	16 in/ 16 out	16 in/ 16 out
Data Buffering	66 word FIFO	NO	NO	NO	NO
Byte Packing	YES	YES	YES	NO	YES
Handshake Modes	Pulsed only	Full, Pulsed Clocked	Full, Pulsed Clocked	Full, Pulsed Clocked	Full or Pulsed
Throughput	4.7 Mbytes/s	500 Kbytes/s	850 Kbytes/s	1 Mbyte/s	65-550 Kbytes/s
Electrical Line Characteristics	Differential, TTL-Pos True or GND True	TTL Pos True or GND True DTL Out	TTL Pos True or GND True DTL Out	TTL Pos True or GND True DTL Out	TTL Pos True or GND True DTL Out
# Control Lines	3	2	4	2	1
# Status Lines	2	2	4	2	1
Interrupt Capability	YES	YES	YES	YES	YES
Parity Lines	2 in/2 out	0	0	0	0

Ordering Information

HP 27114A Parallel Asynchronous FIFO Interface

The HP 27114A includes:

1. Printed circuit assembly (27114-60001).
2. Three metre cable assembly (27114-63001).
3. 96-pin Wirewrap connector kit (27114-60003).
4. Installation & Reference Manual (27114-90001).

27114A Options

0B0: Deletes Installation & Reference Manual (27114-90001).

002: Adds loopback test hood (27114-60002).

003: Deletes 3 meter cable (27112-63001) and adds single-ended positive true/ground true 3 meter cable (27114-63002) and 6 resistor network, SIP, $8 \times 1.5k \times 3.3k$ ohm (1810-0407).

004: Replaces 3 meter differential cable (27114-63001) with 12 meter differential cable (27114-63003)

005: Deletes 3 meter differential cable (27114-63001)

The 96 pin terminated differential cable consists of 48 twisted pair 32 gauge wire wrapped in a combination of foil/braid shield.

The 96 pin terminated single-ended cable consists of 48 28 gauge wires wrapped in a combination of foil/braid shield.

These cables are available from Corporate Parts Center.





Information subject to change without notice.

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