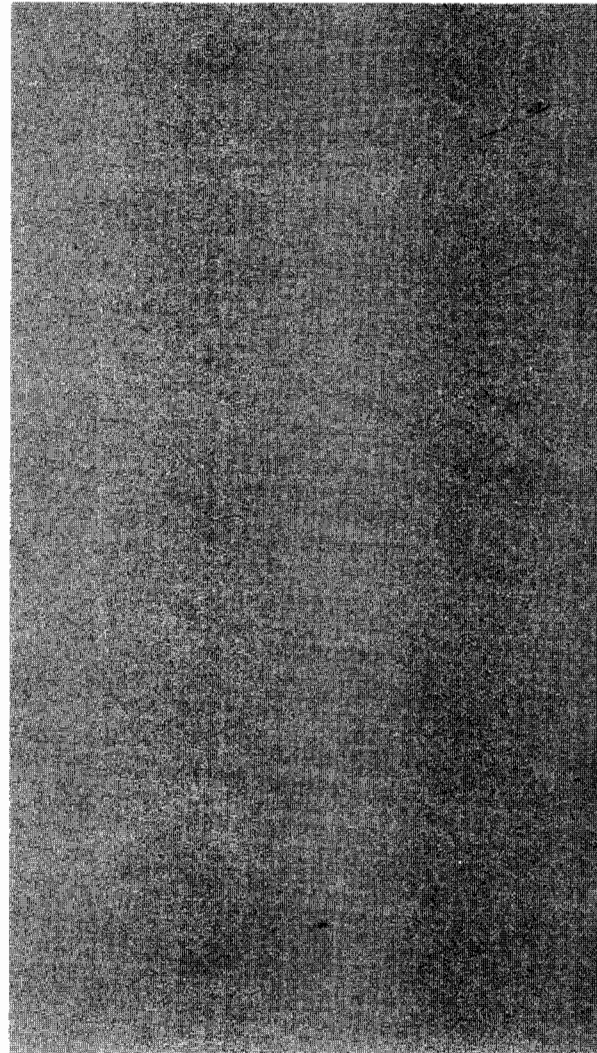


HP Apollo Series 700
Graphics Systems:
*The Graphics Architecture
of the 1990s*



THE GRAPHICS ARCHITECTURE FOR THE 1990s

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The Graphics Architecture for the 1990s



Introduction -- The Waiting is Over

Whether you use commercial applications such as desktop publishing, financial services, or information management retrieval — or technical applications such as mechanical design, scientific visualization, or advanced solids modeling — with HP graphics running on HP Apollo Series 700 workstations, the waiting is over.

HP delivers the fastest X11 performance in the industry, so waiting for your windows to open, close, and do anything in between is a thing of the past. Now you can enjoy immediate response to any of your input, reducing waiting time and improving productivity.

And the same is true for the more technical applications. With outstanding 2D and 3D vector performance and leadership data animation capabilities, now you can design, draw, rotate — perform any graphics task — faster than ever before.

Much of the leadership graphics performance on the HP Apollo Series 700 is due to graphics-specific architectural enhancements to PA-RISC. These enhancements include floating-point instructions that accelerate 2D and 3D transformation calculations and block moving routines in the memory and I/O controller. The tightly coupled CRX architecture is designed for optimum performance at the lowest-possible cost; it accelerates only those graphics routines which remain too complex to handle in a general-purpose CPU.

This ability to leverage the processor also enables access to high-end graphics features from entry-level systems via PowerShade software.

We call the HP CRX graphics architecture the “graphics architecture of the 1990s” because it provides the best customer investment protection of any graphics architecture on the market. These graphics were designed with system growth in mind. When processor performance is improved, graphics performance likewise improves, a process we call “performance scaling.”

Competitive architectures that rely on isolated processors for graphics acceleration find that performance is “locked into” the technology level of their chosen graphics processor. Upgrading the CPU in these types of systems produces few, if any, graphics performance gains. You would need to upgrade both CPU and graphics processors to achieve application performance gains.

Figures 1 and 2 demonstrate the graphics performance increases that result from upgrades to CPU performance. Figure 1 shows the boost in X Window performance as measured by the X11Perf benchmark. Figure 2 highlights the 3D modeling performance improvement as measured by the lighted and shaded quadrilaterals benchmark. It clearly demonstrates how your investment in graphics hardware is protected — regardless of which CRX subsystem is used, graphics performance is boosted as CPU performance increases.

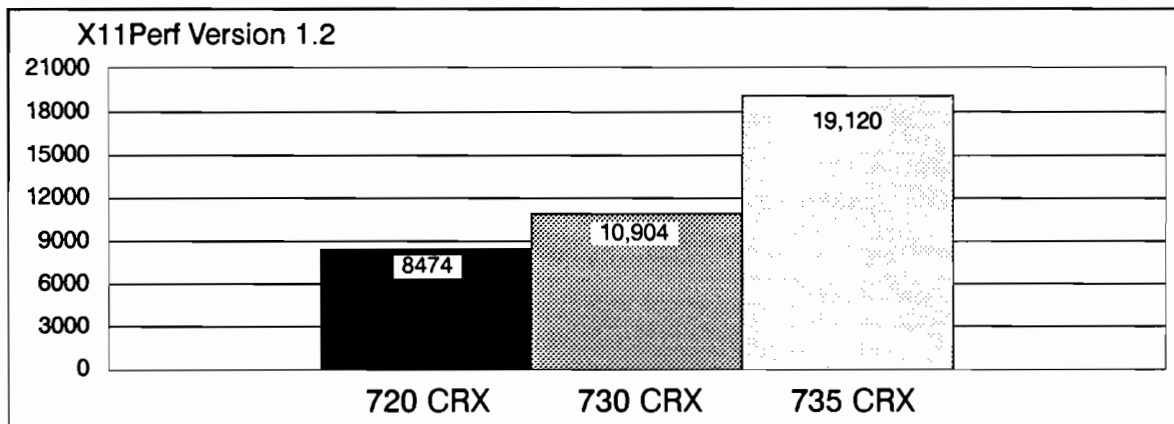


Figure 1: X11Perf Performance Scaling

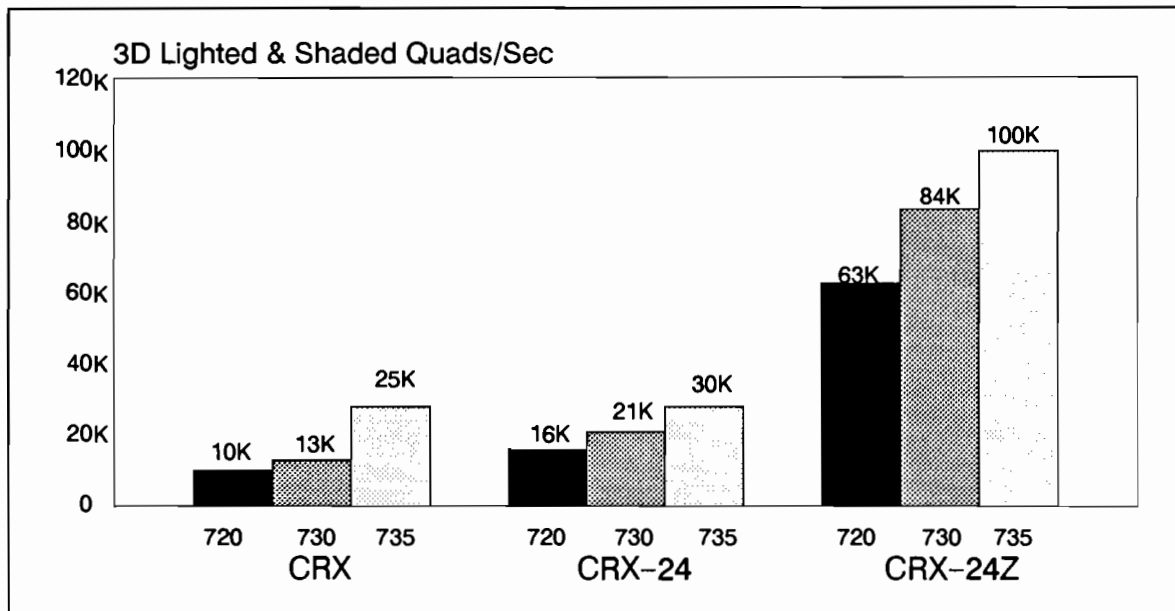


Figure 2: 3D Lighted and Shaded Quads Performance Scaling

CRX Graphics Family Products

HP's CRX graphics provide superior performance in all areas without sacrificing performance in one area at the expense of another. The new CRX-48Z is a case in point: it provides superior vector performance, superior solids-modeling performance, *and* leadership X Window performance.

This section provides information that will help you select the right HP graphics system for your needs.

Hewlett-Packard's CRX Graphics family has been expanded with a new high-end graphics system and new graphics for second-generation Series 700 workstations. Enhancements include:

- 3D solids graphics now available on entry level systems, including X stations
- New CRX-48Z blazing graphics performance on all new Series 700 systems (except 715/33)
- The benefit of scalable graphics performance is fully realized on the 99 MHz systems
- PEX/PEXlib for open, distributed 3D graphics (as X/Xlib does for 2D)

Figure 3 shows the graphics offerings supported on Series 700 workstations.

	715/33 	715/50 	725/50 	735 	755 
Integrated Grayscale	●	●	●		
Integrated 17" 1024x768 Color	●				
Integrated 19" 1280x1024 Color	●	●	●		
GRX Grayscale				●	
CRX Color				●	●
CRX-24	●	●	●	●	●
CRX-24Z	●	●	●	●	●
CRX-48Z		●	●	●	●

Figure 3: Series 700 Workstation Graphics Offerings

715/725 Grayscale *NEW!*

The grayscale graphics of the 715 and 725 feature fast X Window performance with 8-bit images. It is entry-priced to provide high performance with superb value. The 715/725 Grayscale system is appropriate for a wide variety of markets.

715/725 Color *NEW!*

Models 715 and 725 graphics feature fast X Window performance and fast vector performance at entry-level prices. With the addition of PowerShade software, the 715 and 725 Color workstations perform lighting and shading for surface rendering, and allow access to high-end functionality through the Personal Visualizer (from Wavefront Technologies). The 715/725 Color system is appropriate for a wide variety of markets.

GRX (720, 730, 735)

A high-performance grayscale system targeted for cost-conscious customers. GRX is capable of displaying 8-bit images. Typical applications include CASE, artificial intelligence, grayscale imaging, and database management.

CRX (720, 730, 735, 750, 755)

Leadership graphics capabilities in X Window performance and in color vector performance at OVER ONE MILLION vectors per second describe the CRX graphics system. CRX is capable of displaying 8-bit color images with 8+8 double buffering. With the addition of PowerShade software, the CRX can perform dynamic lighting and shading.

CRX-24 (715, 720, 725, 730, 735, 750, 755)

Fast and flexible 24-bit images with excellent X Window performance characterizes the CRX-24 graphics systems. Eight dedicated overlay planes allow nondestructive overlays and superb user-interface performance. The CRX-24 has multiple color maps available and multiple display modes

to meet the most demanding visualization needs. The CRX-24 graphics occupies a single board slot in a 720, 730, 735, 750 or 755 system. It occupies the EISA slot in a 715 or 725 system. In either system it can be upgraded to the CRX-24Z graphics configuration described below. The CRX-24 is a good solution for applications that require double buffering on the entry-level platforms, the 715 and 725.

With the addition of PowerShade software, the CRX-24 can perform dynamic lighting and shading for surface rendering, and fast volumetric rendering. Third-party stereoscopic viewing hardware is supported on the CRX-24. Typical customers for the CRX-24 graphics are in engineering analysis, scientific visualization, earth resources, GIS, and image processing.

CRX-24Z (715, 720, 725, 730, 735, 750, 755)

A 24-bit Z buffer providing fast polygons and anti-aliased lines defines the advantages of the CRX-24Z over the CRX-24 graphics. All the capabilities of the CRX-24 graphics are maintained intact at full performance with these two additional performance improvements. The CRX-24Z graphics occupies a single board slot on a 720, 730, 735, 750 or 755 system. It occupies the EISA slot in a 715 or 725 system.

PowerShade software comes bundled with the Series 700 CRX-24Z systems, providing high-performance lighting and shading capabilities for surface rendering while maintaining fast data animation capabilities.

CRX-48Z (715/50, 725, 735, 755) *NEW!*

48 color planes for true color double buffering, exceptionally fast polygons, and anti-aliased vector performance are the contributions the CRX-48Z makes over the CRX-24Z. The CRX-48Z graphics are delivered in a small cabinet which may sit on or beside the system box. The interface card occupies a single board slot on a 735 or 755 system. It occupies the EISA slot in a 715 or 725 system.

PowerShade software comes bundled with the Series 700 CRX-48Z systems, providing fast data animation capabilities.

Figure 4, on the following page, summarizes HP's graphics offerings on the Series 700 workstation family. Tables 1-3 detail graphics specifications for second-generation Series 700 Models 715, 725, 735, and 755.

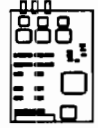
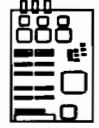
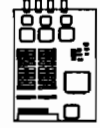
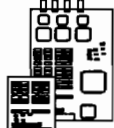
Series 700 Graphics Product Family							
Name:	Grayscale	Color	GRX	CRX	CRX-24	CRX-24Z	CRX-48Z
Physical Packaging:	 <i>Integrated</i>	 <i>Integrated</i>	 <i>Modular: 1 board</i>	 <i>Modular: 1 board</i>	 <i>Modular: 1 board</i>	 <i>Modular: 1 board w/ daughter card</i>	
Abbreviated Product Definition:	- grayscale 8 plane, or 4/4 dbl. buffer	- color 8 plane, or 4/4 dbl buffer 8/8 virtual	- grayscale 8 plane with <u>8/8 dbl buffer</u>	- color 8 plane with 8/8 dbl buffer	- color <u>24 plane</u>, or 12/12 dbl bfr. 8 overlay pls - volumetric rendering	- color 24 plane, or 12/12 dbl bfr. 8 overlay pls - antialiasing <u>h/w Z-buffer</u> <u>accelerated shading</u> - volumetric rendering	- color 48 plane: <u>24/24 dbl bfr.</u> 8 overlay pls <u>hi-perf anti-aliased vectors</u> - h/w Z-buffer <u>accelerated shading</u> - volumetric
with...							
PowerShade							
							
3D Surfaces & Advanced Rendering for color systems	n/a	▪ <u>entry-level shading</u>	n/a	▪ <u>dynamic shading</u>	▪ <u>dynamic shading</u>	-bundled-	-bundled-
Supported by:	715, 725	715, 725	720, 730, 735	720, 730, 735, 750, 755	715, 720, 725, 730, 735, 750, 755	715, 720, 725, 730, 735, 750, 755	715/50, 725, 735, 755
Target Markets:	Desktop Publishing CASE Desktop Productivity Info. Mgmt. & Retrieval	EDA (schematic capture) Mechanical CAD (drafting, 2D design) AEC 2D CASE Commercial	Desktop Publishing CASE Desktop Productivity Info. Mgmt. & Retrieval	EDA Mechanical CAD Mech. CAE (Low-End) Financial Services GIS Scientific Analysis	Sci. Analysis Visualization Imaging Earth / Energy Resources GIS	M CAD/MCAE (Solids Modeling and Analysis) Sci. Visualization (Adv. Analysis and Visualization) AEC (visualization & walk-throughs)	MCAD/MCAE (Adv. Solids Modeling, Design Concept) Sci. Visualization (Adv. Analysis and Visualization) AEC (visualization & walk-throughs)

Figure 4: CRX Graphics Product Family

Table 1: Models 715 and 725 Graphics Specifications

	Grayscale/Color		CRX-24		CRX-24Z		CRX-48Z
Image Planes Z Buffer Planes Overlay Planes Double Buffer Planes Resolution Monitor Size Scan Rate	8 0 0 4/4 1024x768 or 1280 x 1024 17" or 19" 75Hz or 72Hz		24 0 8 12/12 1280 x 1024 19" 72Hz		24 24 8 12/12 1280 x 1024 19" 72Hz		48 24 8 24/24 1280 x 1024 19" 72Hz
X Benchmarks	Model 715/33	Model 715/50 725/50	Model 715/33	Model 715/50 725/50	Model 715/33	Model 715/50 725/50	Model 715/50 725/50
X11 Perf* Vectors/sec (sustained) Rectangles/sec Char/sec	7,633 589,000 312,000 186,000	11,190 859,000 341,000 313,000	7,424 555,000 263,000 201,000	10,650 804,000 282,000 289,000	7,424 555,000 263,000 201,000	10,650 804,000 282,000 289,000	9,890 803,000 547,000 279,000
2D Benchmarks							
Memory to Display Transfer Rates (8 bit Pixels/sec) Screen Clear Time	20M 9.4	28M 9.4	4.95	4.95	4.95	4.95	30M 2.55
3D Benchmarks							
3D Vectors/sec 3D Antialiased Vecs/sec (sust.) 3D Triangles/sec (sust.) 3D Lighted Quads/sec (sust.) Volumetric Rendering (Voxels/sec)	810K N/A 12K 10K N/A	920K N/A 18K 10K N/A	810K N/A 12K 8K 2M	680K N/A 18K 12K 3.5M	810K 150K 100K 50K 2M	680K 150K 150K 70K 3.5M	1,000K 1,000K 600K 80K 3.5M
Color Only							
GPC Benchmarks**							
3D Wireframe (sys_chassis) 3D Solids (cyl_head) 3D Animation (head) 3D simulation (shuttle)	12.80 9.30 13.60 10.50	19.10 14.20 20.90 16.00	12.00 9.70 13.10 10.60	19.00 14.70 21.10 16.10	12.00 23.10 27.10 17.50	19.00 34.20 40.30 26.30	21.79 39.56 66.70 26.34
Color Only							

Requires PowerShade Software

*A combined X benchmark based on The Digital Review Methodology (5/7/90 issue, p.44).

**A ratio of a series of benchmarks by NCGA. See Chapter 3 for more information on GPC.

All 3D Performance is measured through Starbase. PEXlib and HP-PHIGS delivers similar performance.

Table 2: Models 735 and 755 Graphics Specifications

	GRX (735 only)	CRX	CRX-24	CRX-24Z	CRX-48Z
Image Planes	8	8	24	24	48
Overlay Planes	0	0	8	8	8
Double Buffer Planes	8/8	8/8	12/12	12/12	24/24
Z Buffer Planes	0	0	0	24	24
Resolution	1280 x 1024	1280 x 1024	1280 x 1024	1280 x 1024	1280 x 1024
Monitor Size	19"	19"	19"	19"	19"
Scan Rate	72Hz	72Hz	72Hz	72Hz	72Hz
X Benchmarks					
X11 Perf*	19,120	19,120	18,790	18,790	19,120
Vectors/sec (sust.), 10 pixel	971,000	971,000	652,000	652,000	1,240,000
Rectangles/sec, 10x10	287,000	287,000	301,000	301,000	757,000
Char/sec TR10 font, 80	543,000	543,000	400,000	400,000	514,000
2D Benchmarks					
Memory to Display Transfer	39,000,000	39,000,000	39,000,000	39,000,000	40,000,000
Rates (8-bit pixels/sec)	9.4 msec	9.4 msec	4.95 msec	4.95 msec	2.55 msec
Screen Clear Time					
3D Benchmarks					
3D Vectors/sec	1,160,000	1,160,000	680,000	680,000	1,900,000
3D Antialiased Vecs/sec (sust.)	N/A	N/A	N/A	150,000	1,200,000
3D Triangles/sec (sustained)	N/A	40,000	40,000	175,000	600,000
3D Lighted Quads/sec (sust.)	N/A	25,000	30,000	95,000	150,000
Volumetric Rendering (Voxels/sec)	N/A	N/A	7,000,000	7,000,000	7,000,000
GPC Benchmarks					
ECAD (pc_board)	N/A	N/A	N/A	N/A	N/A
3D Wireframe (sys_chassis)	N/A	32.50	33.50	31.20	40.30
3D Solids (cyl_head)	N/A	34.00	34.00	57.10	78.74
3D Animation (head)	N/A	41.00	41.00	69.00	127.05
3D Animation (shuttle)	N/A	38.00	38.65	50.20	58.51

Requires PowerShade Software

N/A - not available

*A combined X benchmark based on The Digital Review Methodology (5/7/90 issue, p 44).

All 3D Performance is measured through Starbase; PEXlib and HP-PHIGS delivers similar performance.

Table 3: Series 700 Color Graphics Features

	Model s 715, 725 Color		CRX		CRX-24		CRX-24Z	CRX-48Z
Graphics Features		PowerShade		PowerShade		PowerShade	PowerShade	PowerShade
CPU Integrated Graphics	✓	✓	✓	✓	✓	✓	✓	✓
Hardware Cursor	✓	✓	✓	✓	✓	✓	✓	✓
HW BLT	✓	✓	✓	✓	✓	✓	✓	✓
HW Text Acceleration	✓	✓	✓	✓	✓	✓	✓	✓
Virtual True Color (Dithering)	✓	✓	✓	✓	✓	✓	✓	✓
Screen Door Transparency	○	✓	○	✓	○	✓	✓	✓
Alpha Blending Transparency	○	○	○	○	○	✓	✓	✓
Depth Cuing	✓	✓	✓	✓	✓	✓	✓	✓
Antialiasing	○	○	○	○	○	○	✓	✓
Gamma Correction*	○	✓	○	✓	○	✓	✓	✓
Gouraud Shading	○	✓	○	✓	○	✓	✓	✓
Phong Lighting	○	✓	○	✓	○	✓	✓	✓
Radiosity	○	✓	○	✓	○	✓	✓	✓
Raytracing	○	✓	○	✓	○	✓	✓	✓
Deformation Animation*	○	✓	○	✓	○	✓	✓	✓
Polygon Mesh	✓	✓	✓	✓	✓	✓	✓	✓
6-Axis Interpolation	○	✓	○	✓	○	✓	✓	✓
6th Order Nurbs	✓	✓	✓	✓	✓	✓	✓	✓
Sectioning, Capping*	○	✓	○	✓	○	✓	✓	✓
Interference Checking*	○	✓	○	✓	○	✓	✓	✓
Stereo Display Support*	○	○	○	○	✓	✓	✓	✓
Voxel Primitive*	○	○	○	○	✓	✓	✓	✓
Pattern Area Fill*	✓	✓	✓	✓	✓	✓	✓	✓
Display List Picking	✓	✓	✓	✓	✓	✓	✓	✓
Graphics Application Interface								
X11 R5	✓	✓	✓	✓	✓	✓	✓	✓
PHIGS	✓	✓	✓	✓	✓	✓	✓	✓
PEX	○	✓	○	✓	○	✓	✓	✓
Starbase	✓	✓	✓	✓	✓	✓	✓	✓
Personal Visualizer	○	✓	○	✓	○	✓	✓	✓

○ = not supported
* Starbase API only

Entry Level Multimonitor (715, 725) *NEW!*

The CRX-24 on the Model 715 and Model 725 provides a very cost-effective solution to most dual-monitor applications. Customers who purchase the CRX-24 option need only add a second monitor to take advantage of the integrated 8-bit color subsystem on the system motherboard.

Dual CRX (720, 730, 735, 750, 755)

Dual CRX graphics provides multimonitor, single-user CRX graphics on a 720, 730, 735, 750, or 755 system. The Dual CRX graphics occupies a single system slot and provides two high-performance CRX displays of 8 bits each (also supporting 8+8 double-buffering). PowerShade software is supported on Dual CRX graphics.

For added capabilities, the Model 750 can support two Dual CRXs, for a maximum four displays, or two CRX-24s for two 24-plane true-color displays.

Typical applications where customers might use multimonitor systems are GIS, Command and Control, financial transaction processing, and process control.

Figure 5 below reviews the multimonitor graphics offerings.

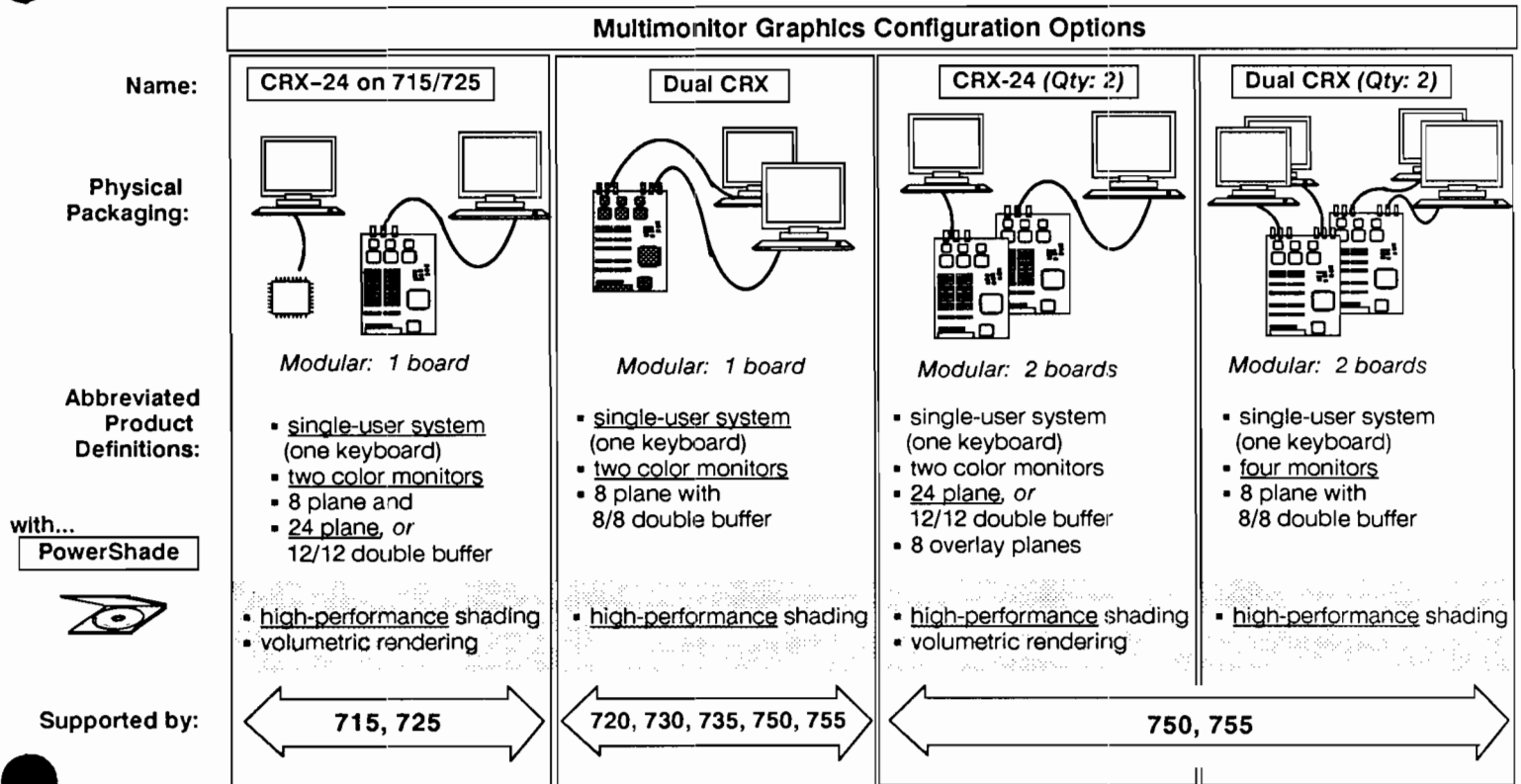
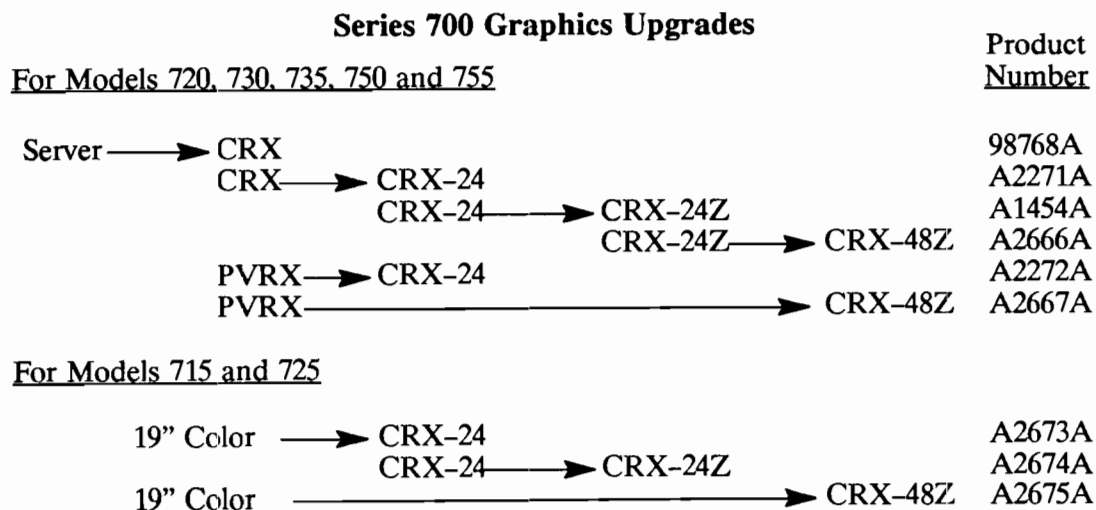


Figure 5: Multimonitor Graphics Configuration Options

Graphics Upgrades

The modular design and compatibility of the CRX graphics make upgrades within the Series 700 family attractive in those cases when application demands grow beyond the originally purchased system.



Industry Dynamics

PEXlib/PEX, Open GL, PHIGS, XGL, Starbase, and other graphics application programming interfaces (APIs) are receiving a lot of attention in the trade press. One reason is that the industry is looking for an open, industry-standard graphics API that meets the needs of today's client-server environment. At the same time, developers want the same level of performance in a standards-based API as in a proprietary API. HP delivers just that — full performance graphics APIs through standards. In the following section, we will discuss the industry trends regarding APIs, as well as HP's graphics API strategy, and the position of HP's graphics API products.

HP is the X Window Performance Leader

HP's Series 700 has provided the highest-performance systems for running the X11 R5 Window System — not at one price point, but AT EVERY PRICE POINT! Our lead in this area is so strong that in many cases, our ENTRY systems can outperform the BEST systems that our competition can offer!

Why is this important? The X11 network protocol is the defacto standard of the industry. By default, the display calls of X11, known as "Xlib," constitute the most portable 2D graphics library in the world. AND HP RUNS THIS MOST-PORTABLE 2D GRAPHICS LIBRARY THE FASTEST OF ANYONE — ON ALL OUR PRODUCTS!! X11 performance affects 3D applications also in that it speeds the user interface.

Industry-Standard Graphics Libraries (APIs)

As shown in Figure 6, the industry is moving away from proprietary, standalone solutions such as HP's Starbase and SGI's GL, to one based on an open, standards-based, client/server model. In the 2D world, this has already happened with X, Xlib and Motif. Every major workstation vendor has adopted the X Window System, even though they had to abandon their own proprietary solution. The industry is following the same trend in the 3D world with PEX and PEXlib (as shown in Figure 7). HP, Sun Microsystems, IBM, DEC, and a host of others have publicly announced support for PEX and PEXlib. In fact, several vendors, including HP, are already shipping PEX-based products.

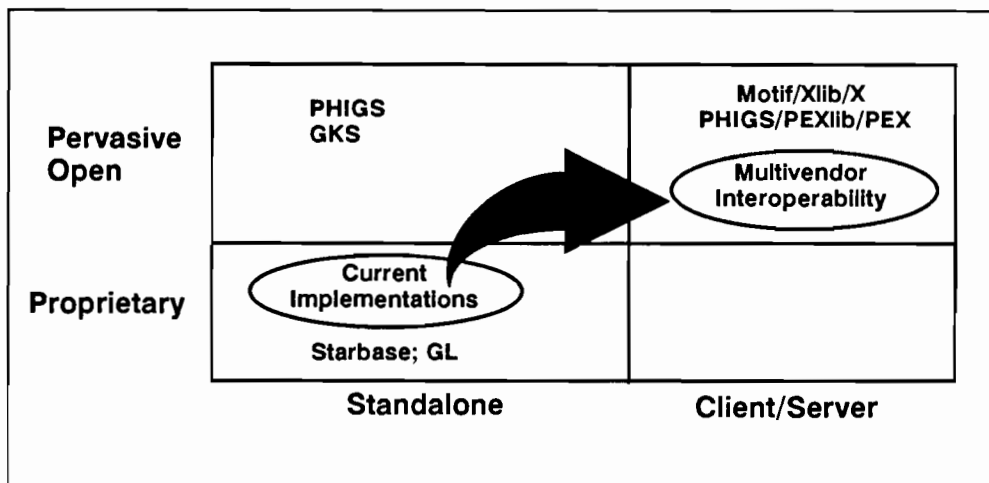


Figure 6: Graphics API Market Trends

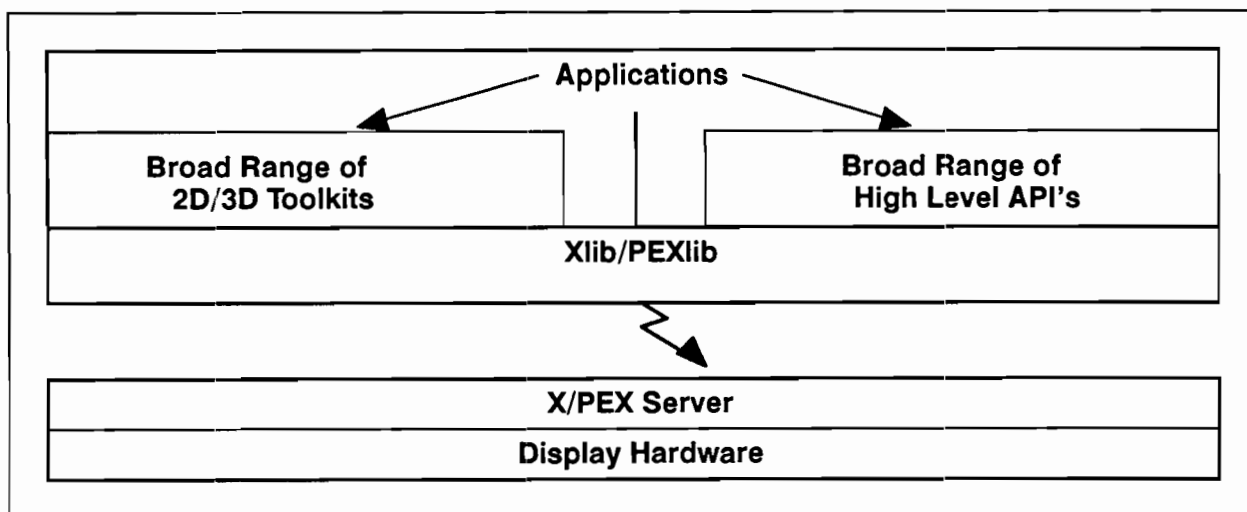


Figure 7: The Xlib/PEXlib Solution -- Open Client/Server Graphics API Architecture

HP Provides Full Performance Through Standards

Among developers and end users, several common themes emerge regarding graphics APIs. First and foremost is performance. There is a belief that a standards-based solution means the application will run slower. NOT TRUE!!! While some vendors chose to structure their standards-based APIs on top of their proprietary API (in which case they do run slower), HP provides a native implementation of its PHIGS and PEX-based software products. In addition, when the application is running locally, HP's standards-based API solutions (PHIGS and PEX) directly access the hardware (DHA) providing a level of performance that is equivalent to HP's Starbase library which leads the industry in X Window performance).

Note that the performance quoted in Tables 1 and 2 is for PEXlib, HP-PHIGS, and Starbase. Because of their niche market positioning, SGI invests heavily in tuning for graphics performance, rewriting low-level code and targetting their graphics accelerators. One of the drawbacks of this approach is that applications must be able to take full advantage of the hardware capabilities. The advent of high-performance CPU's like PA-RISC, with integrated floating point and instruction sets that support graphics rendering, have made hardware accelerators unnecessary for many applications.

The next common theme brought out by developers is portability and interoperability. Developers want portable applications. This means an application developed using PEXlib on a DEC system can move over to an HP system and run with minimal recoding. The benefit to the developer is obvious — a reduction in software engineering support and faster time to market. Interoperability is important to the end user as well as the developer. Applications written to PEXlib and running on a Sun system can interoperate with an HP system. In other words, the application will run on the Sun system, but an HP system will be used to display and interact with the application. As a result, the end-user has access to a greater number of applications as well as a wider choice of hardware solutions — from PEX terminals to PEX compute servers. It's important to note that three companies today provide PEX terminals. There are NO GLX terminals available in the market. This is another reason why the industry requires a single 3D protocol.

The final common theme brought out by developers is ease of use. Again their reasons are straightforward: time-to-market constraints, reduction in resources, and so on. For developers

who have programmed in Xlib, the 2D low-level API, they will find PEXlib a natural extension (Xlib/PEXlib were developed by the M.I.T. X Consortium). In addition, PEXlib shares many of the same semantics as PHIGS, therefore, developers who have programmed in PHIGS will feel comfortable with it. HP's implementation of the PEXlib standard has a unique differentiator to help developers get up and running as fast as possible — on-line hypertext. HP has worked with O'Reilly and Associates, the industry standard when it comes to X-based reference books, to provide a PEXlib on-line tutorial, complete with programming examples and a hypertext help facility.

Industry Support for PEX

The PEX Interoperability Center (PEX IC) — near Dallas officially opened February 1992. It provides members of the PEX consortium with facilities for PEX interoperability testing. By contributing and maintaining up-to-date hardware and software at the Center, members may participate in testing activities at no charge for the first year. Group testing activities enable members to prepare interoperability demonstrations. The Center also provides a convenient alpha or beta test site for new PEX products and releases. Additionally, the SIGGRAPH interoperability demonstrations ensure that moving applications from vendor to vendor will really be possible.

PEX IC members as of September 1992 include: Advanced Technology Center, Advanced Visual Systems, Inc., Convex Computer Corp., Data General Corp., Digital Equipment Corp., Evans & Sutherland, Fujitsu Ltd., Hewlett-Packard Co., Liant Software Corp., Media Metrix Inc., MIT X Consortium, Network Computing Devices, Oki Electric Industrial, Omron Corp., O'Reilly & Associates Inc., SHOgraphics, Sun Microsystems, and Tektronix. In addition to the PEX IC in Dallas, companies in Japan are working to open their own Center.

HP's 3D Graphics API Strategic Direction

HP's graphics API program can be divided into two types, strategic and third party. HP's strategic or internally developed APIs strengthen HP's scalable architecture strategy through a device-independent implementation. The result is that HP's 3D APIs run on all of HP's 3D Series 700 systems. Furthermore, when HP PowerShade is added, you can run your application remotely to an X station.

For customers moving into a distributed 3D environment HP offers a choice of solutions (see Figure 8), including a local client-server implementation using direct hardware access, a remote 3D solution via X, and a remote 3D solution via PEX.

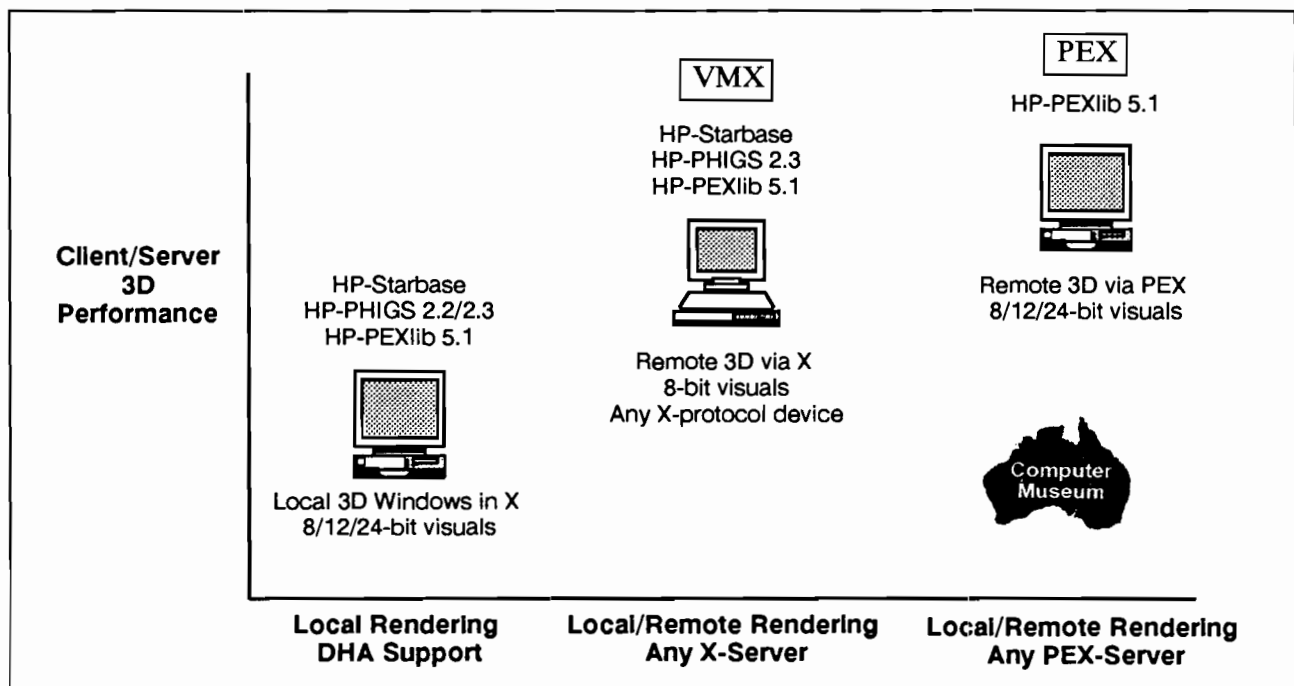


Figure 8: HP's 3D Graphics API Strategy

HP's strategic APIs include:

- HP Starbase—proprietary API for local 2D/3D and remote 2D/3D via X. There are no plans to provide PEX support via Starbase.
- HP PHIGS—ANSI/ISO-based API for local 2D/3D and remote 2D/3D via X. HP is planning to provide PEX support via PHIGS sometime next year
- HP PEXlib—MIT X Consortium-based API for local 2D (X-lib)/3D and remote 2D/3D via X or PEX. For developers who today require full-performance, distributed 3D graphics, HP PEXlib/PEX is the right solution.

In addition to full performance, HP's strategic APIs are the first with new functionality, tightly integrated with HP's hardware and software, part of HP's worldwide support program, and have HP's long-term commitment for full support on HP platforms. In other words, HP's strategic APIs are the recommended APIs for software developers.

The third-party APIs are supported through HP's Channel Partners and include the following:

- ATC-GKS by Advanced Technology Center — an ANSI-based multivendor API
- FIGARO by LIANT Software — an ISO-based multivendor API
- HOOPS by Ithaca Software — an object-oriented graphics programming language
- Nth Portable GL by Nth Graphics—a GL 4.0 on Starbase software package

New HP Graphics Software

What's New

Listed below are the new graphics API products from HP:

- HP-PEX 5.1 3D Development Environment includes direct hardware access (full-performance) capabilities as well as on-line hypertext and hardcopy documentation.
- HP-PHIGS 2.3 adds remote 3D graphics via X, which means you can run HP PHIGS on your X terminal. And to make programming easier, HP-PHIGS 2.3 adds support for the PHIGS Motif drawable widget.

- PowerShade software enables 3D visualization on any Series 700 color workstation.
- HP ARTCore allows creation of highly realistic (“photorealistic”) images using HP’s leadership radiosity and ray-tracing technology.

These new products, and a host of other HP products, are described below in more detail.

HP-PEX 5.1

HP-PEX 5.1 ordering information:

B3176A HP-PEX 5.1 3D Development Environment License-to-use HP-PEX client-server development libraries for one Series 700 workstation. For use with HP-UX version 9.0. Supports the CRX-48Z and CRX-24Z through bundled PowerShade software. Supports the Series 700 Color, CRX and CRX-24 ONLY when optional HP PowerShade is present. This product includes the B3177A HP-PEX 5.1 Run-

B3177A HP-PEX 5.1 Run-Time Libraries License-to-use HP-PEX client/server run-time libraries for one Series 700 workstation. For use with HP-UX version 9.0. Supports the CRX-48Z and CRX-24Z. Supports Series 700 Color, CRX and CRX-24 ONLY when HP PowerShade is present. Order the APH option and the same number of media options (either AAH or AAU).

HP-PHIGS 2.3

HP-PHIGS 2.3 ordering information:

B2363D HP-PHIGS 2.3 Development Environment License-to-use HP-PHIGS 2.3 development libraries for one Series 700 workstation. For use with HP-UX version 9.0. Supports all Series 700 graphics subsystems. This product includes the B2364D HP-PHIGS Run-Time Libraries.

B2364D HP-PHIGS 2.3 Run-Time Libraries License-to-use HP-PHIGS 2.3 runtime libraries for one Series 700 workstation. For use with HP-UX version 9.0. Supports all Series 700 graphics subsystems.

Note: HP PowerShade must be present (bundled with 24Z and 48Z graphics) to obtain Gouraud Shaded and lit images and hidden surfaces capabilities.

PowerShade [B2156B]

It consists of two distinct parts: software algorithms for 3D lighting and shading and The Personal Visualizer from Wavefront Technologies. The PowerShade software allows entry color workstation users the option of performing 3D solids-modeling through software with good performance — a capability only delivered in hardware on competitive systems! For example, PowerShade software can be added to the 715 Color workstations to enable realistic-looking 3D objects instead of traditional wireframe objects drawn with lines. The capabilities that PowerShade adds to a Series 700 color graphics system are summarized in Table 4.

Table 4: Graphics Capabilities with PowerShade		
System	Base Capability	Capability with PowerShade
700/RX Stations	2D via X	3D for very cost sensitive applications
715/725 Color	Entry Wireframe	Entry Lighting and Shading
S700 CRX S700 Dual CRX	Leadership Wireframe	Dynamic Lighting and Shading
S700 CRX-24	Leadership Wireframe True Color Imaging	Dynamic Lighting and Shading Dynamic Volume Rendering
S700 CRX-24Z	N/A (PowerShade bundled)	Leadership Wireframe High-performance Lighting, Shading Dynamic Volume Rendering Dynamic Antialiasing
S700 CRX-48Z	N/A (PowerShade bundled)	Premier Wireframe Premier-performance Lighting, Shading Premier Volume Rendering Premier-Performance Antialiasing

PowerShade's algorithms for 3D lighting and shading are available to application developers through the following graphic APIs: Starbase, HP-PHIGS and HP's PEXlib. If the application developer has accessed these algorithms in code, customers using that application can automatically enable 3D solids-modeling capability by purchasing PowerShade software (B2156B) as an option for their systems. PowerShade software is bundled on all CRX-24Z and CRX-48Z systems. It is an option available for users of CRX, CRX-24 and entry "Color" system users. It is not supported for use on grayscale systems.

The second part of PowerShade software is The Personal Visualizer, a visualization application from Wavefront Technologies. The Personal Visualizer enables ANY customer to create photo-realistic 3D scenes (using radiosity and ray-tracing), perform interactive "walk-throughs," and show objects in motion (using key-frame animation). The Personal Visualizer incorporates numerous features from its Advanced Visualizer application and represents a unique value to the visualization-minded customer. Any customer who purchases PowerShade software has immediate access to this visualization capability.

Figure 9 below shows the two distinct parts supplied by PowerShade software and some of the benefits provided.

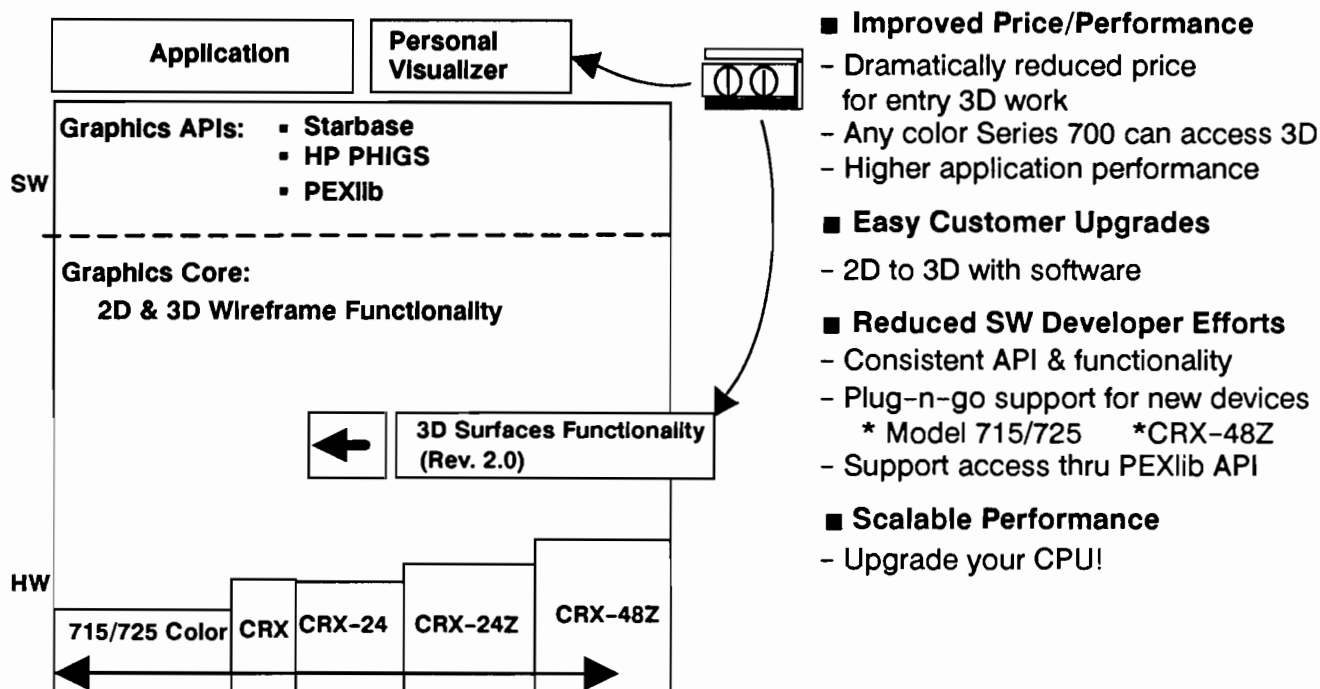


Figure 9: PowerShade (Rev. 2) Benefits

ARTCore (Advanced Rendering Technology Core) [B2930A & B2931A]

HP ARTCore is a library for 3D application developers that allows them to create highly realistic ("photorealistic") images within their applications using HP's leadership radiosity and ray-tracing technology. The HP ARTCore product can be used with any supported 3D graphics library (i.e., Starbase, PEXlib, third-party GL) on an HP system. Development licenses [B2930A] are available to application developers using HP platforms. Run-time licenses [B2931A] are available to customers using these applications on HP platforms. This technology (encrypted source code) can be licensed for use on non-HP platforms.

HP VUE 3.0 **IMPROVED******

HP Visual User Environment (HP VUE) is a graphical user interface based on the Motif environment and bundled with every Series 700 workstation. HP VUE is used to integrate multimedia technologies to make them more useful to the end user. With HP VUE's mouse-driven, icon-based, drag-and-drop model of interaction, a user can quickly and easily access information on local and remote computers.

HP VUE has six primary components that give novice and expert UNIX users easy access to the power of UNIX:

- Login Manager provides a graphical way to begin a work session.
- File Manager lets the user navigate through directories on local and remote computers. Using the mouse, files or directories can be moved, copied, deleted, and renamed. Double-clicking a data file icon automatically launches the appropriate application.
- Workspace Manager provides multiple workspaces, which is like having multiple monitors for a user's applications. The Workspace Manager also has a set of personal productivity and system utilities, such as an Icon Editor, Text Editor, and audio file annotator, that are accessed through buttons and slide-up panels.
- Style Manager lets users customize colors, backgrounds, fonts, and other system settings.

- Session Manager allows the user to log in and find everything exactly how it was left when the user last logged out.
- Help Manager is a system-wide, context-sensitive help system with hypertext and hypergraphics. Applications, including custom applications, can use the Help Manager to display help information.

HP SharedX 2.0 [B2305L] *IMPROVED*****

HP SharedX is a real-time communications product that extends the industry-standard X Window System to allow sharing of X-based applications between two or more remote users or displays. By sharing the application window, all communicators can see and directly edit the original information in the document. This streamlined method of communication is unmatched in the industry.

Sharing can occur at any time and without any changes to most existing X applications. Combined with the telephone, HP SharedX greatly enhances the collaboration that must occur within project teams, especially teams that are geographically dispersed.

HP SharedX substantially increases critical communication and interaction in areas such as timely team decisions and highly responsive technical support. Using HP SharedX, two or more remote users can share and interact directly with the information in X-based application, passing windows and images around the office or around the world. Only the sender needs to be running HP SharedX. Receivers can run standard X or non-X applications on their workstation or X terminals.

HP SharedPrint/UX [B2154A] *NEW*****

HP SharedPrint/UX is an easy-to-use, drag-and-drop printing service that allows users to print color, text, graphics, and images to local or remote printers across the network. It supports laser printers, color ink-jet printers and large format plotters. HP SharedPrint/UX can print Starbase images to either PCL or PostScript compatible printers and provides on-the-fly conversion between PCL to PostScript. It also supports CGM, X bitmaps and TIFF file formats. This frees the user from worrying about what printing format is being used.

The HP SharedPrint/UX user interface allows users to make print requests and control print job parameters and options, queue status, and printer set up and configuration. HP SharedPrint/UX provides integration with the HP Systems Administration Manager (SAM) for printer set-up and configuration.

HP DeskScan/UX [C1788A] *NEW*****

HP DeskScan/UX software supports the HP ScanJet IIc color scanner, allowing users to scan, view, manipulate, store, and print color and monochrome images. HP DeskScan/UX allows manipulation of image scale, brightness, and contrast, with changes seen immediately on the screen. HP DeskScan/UX supports the Automatic Document Feeder for multiple page input. No other workstation vendor currently offers a desktop color scanning solution.

Audio

HP provides an audio annotator that allows end users to audio annotate files, play back audio files, and create audio objects. Using HP's audio API, application programs can utilize the audio capabilities of the Series 700 workstations in a client/server networked environment. The Series 700 Models 715, 725, 735, and 755 include CD-quality hardware, and Models 705 and 710 support voice quality sound.

Applications can use the audio libraries and API to play, record, copy, and edit audio files. Audio file type conversion provides compatibility with other systems. Continuous data streams are supported so that applications can play or record directly from or to an audio device like a cassette player without having to go through data files.

Image

The image viewer allows users to view and manipulate images, including FAX messages. The image library supports industry standard image types, including GIF, TIFF, JPEG, Starbase, Xwd, Xbm, and Xpm. The image developers toolkit allows developers to extend the file types for custom image file formats, and write or display manipulated images to multiple destinations.

With the industry-leading performance of the Series 700, image operations can be done via software, avoiding the additional expense of specialized add-on hardware. For example, the image library includes image compression algorithms, such as JPEG, which run faster on the Series 700 than on competing workstations. This eliminates the need for additional specialized hardware and represents a cost savings over other competitive workstations.

HP RasterOps VideoLive [Z1100A]

HP's RasterOps VideoLive software supports video-in-a-window technology on any graphics top on the Series 700 models equipped with an EISA slot for the HP RasterOps VideoLive EISA board. Users can view live full-motion video in photorealistic color or greyscale. The HP RasterOps VideoLive card supports connection with composite video, S-Video or RGB cables, enabling it to show video from a variety of sources such as TV tuners, VCRs, camcorders, RGB cameras, and medical scanners.

HP RasterOps VideoLive includes a frame grabber that allows users to capture video frames in full 24-bit color for play back or to be saved as TIFF files for use in electronic publishing documents, printing hardcopy, or sending over the network.

Glossary of Graphics Terminology

API (Application Programming Interface) is the graphics library, or set of programming procedures used by the application developer to access the drawing capabilities of the workstation. One big advantage of the X Windowing System and the X/PEX protocol is that it is API neutral. For example, the X protocol can support different high-level APIs or toolkits such as MOTIF and Open Look. The PEX protocol also supports multiple APIs. Application developers and end-users have a choice. This is NOT true with Open GL/GLX. With GLX you are locked into GL.

GLX (GL 4.0 extensions to the X Window System) is SGI's alternative to the PEX protocol. GLX is NOT endorsed or developed by the X Consortium.

GLW (GL extensions to the NT Windowing System) is still undefined. According to SGI, Microsoft has not defined the protocol requirement. Once defined, SGI will write the GL extension for NT.

Low-level vs High-level APIs. Low-level APIs tend to provide basic capabilities through direct access to hardware features (see Figure 7). Because they make no assumptions on how hardware features will be used, they tend to be applicable to a wide range of applications and markets. High-level APIs provide a simpler way to perform complex tasks. They typically derive their functionality from a lower-level API. High-level APIs are typically based on the needs of a particular application class. For example, PHIGS is being tuned to the mechanical CAD market. Typically a market starts with a low-level implementation (e.g., Xlib) and as the market matures, high-level APIs begin to appear (e.g., MOTIF). PEXlib is a low-level, hardware-independent API and HP's PEXlib/PEX 5.1 product is a full-performance implementation of the standard. Open GL is a low-level API and is tied directly to the SGI graphics pipeline. Systems that support a dual API strategy (PEXlib and GL) typically require two graphics pipelines. The result is higher system and support costs as well as higher R&D costs. The payback for a dual API strategy has yet to be proven.

Open GL, previously called GL 5.0, is a rewritten version of SGI's proprietary, low-level GL API. To update from GL 4.0 to Open GL requires a full application port. Open GL will be available sometime in 1993.

PEX, developed by the M.I.T. X Consortium, is the "3D Protocol Extensions to the X Window System". The PEX standard supports immediate-, structured-, and mixed-mode rendering. HP's implementation is based on the PEX 5.1 standard.

PEXlib, developed by the M.I.T. X Consortium, is a low-level application programmer's interface, or library, to the PEX protocol. HP's implementation is based on the current PEXlib (PEX 5.1) standard.

PHIGS (Programmer's Hierarchical Interactive Graphics System) is a high-level, international standard (ISO) programming library for 3D graphics with broad acceptance in the mechanical CAD industry.

Protocol defines how the network information (packets) should be structured. X is the standard protocol for 2D and PEX is the standard for 3D.



Larry J. Thayer

Engineer/Scientist
Hewlett-Packard Company
User Interface Technology Division
3404 E. Harmony Rd.
Fort Collins, Colorado 80525

ABSTRACT

New architecture advances and refinements to existing architectures are fueling continued improvement in 3D graphics workstations. While to date most workstation vendors offer products which implement only traditional architectures, some have introduced products with advanced architectures which take advantage of special graphics features of the CPUs. These new architectures, coupled with increased CPU performance, not only provide superior price/performance, but also broaden both the price and graphics performance range of available workstations.

INTRODUCTION

3D graphics workstations are becoming increasingly sophisticated to meet the growing needs of workstation users. One way this increasing sophistication is presenting itself is in the system architectures employed to provide interactive 3D graphics. When microprocessor performance was relatively limited, interactive graphics performance could be achieved only through the use of custom graphics hardware. Graphics products from a number of vendors show how good performance can be achieved without a fast CPU.

Recently, however, some extremely powerful microprocessors have been described which can provide interactive solid images without special hardware acceleration [Forsyth, DeLano]. With such a processor, it is possible to build a workstation that can not only deliver interactive solid images without special-purpose hardware, but can support a broad range of price/performance points with varying amounts of added hardware. A user of a system would thus be able to select the architecture which delivers as much performance as his budget would allow.

Further performance gains can be achieved by customizing the CPU instruction set and support hardware to enable the CPU to perform graphics operations more efficiently [Dowdell]. Such enhancements can double the performance in some situations without increasing the cost of the system. Most current processors do not have special graphics enhancements, but it is likely more will as processor architectures evolve.

ARCHITECTURE POSSIBILITIES

In order to understand how price and performance of a graphics system can be scaled, it is important to understand an implementation of the graphics pipeline. Figure 1 shows an illustrative partitioning of the pipeline:



Figure 1. 3D Graphics Pipeline for Shaded, Z-buffered Polygons

User graphics data refers to the raw geometric data which defines the image to be drawn. Geometry operations include transformations, lighting and clipping operations. Edge setup is the process which includes decomposing the polygons and calculating edge slope values. Span setup (see Figure 2) is the step where the endpoints of the polygon pixel rows are determined. Pixel interpolation is the part of the pipeline where individual pixel colors are determined and where Z buffering for hidden surface removal takes place.

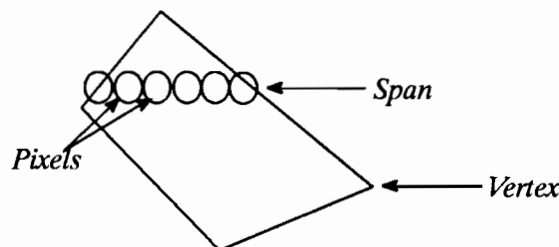


Figure 2. Polygon rendering

The graphics pipeline can be implemented with various mixtures of CPU software and special-purpose hardware acceleration. When implementing the graphics pipeline entirely in software, the CPU would spend most of its time in the latter stages of the pipeline. This is because typically polygons are composed of several spans and each span consists of a number of pixels. Figure 3 shows approximately how much CPU time would be spent in various parts of the pipeline for the case of 100-pixel, lighted, Z-buffered, 3D quadrilaterals.

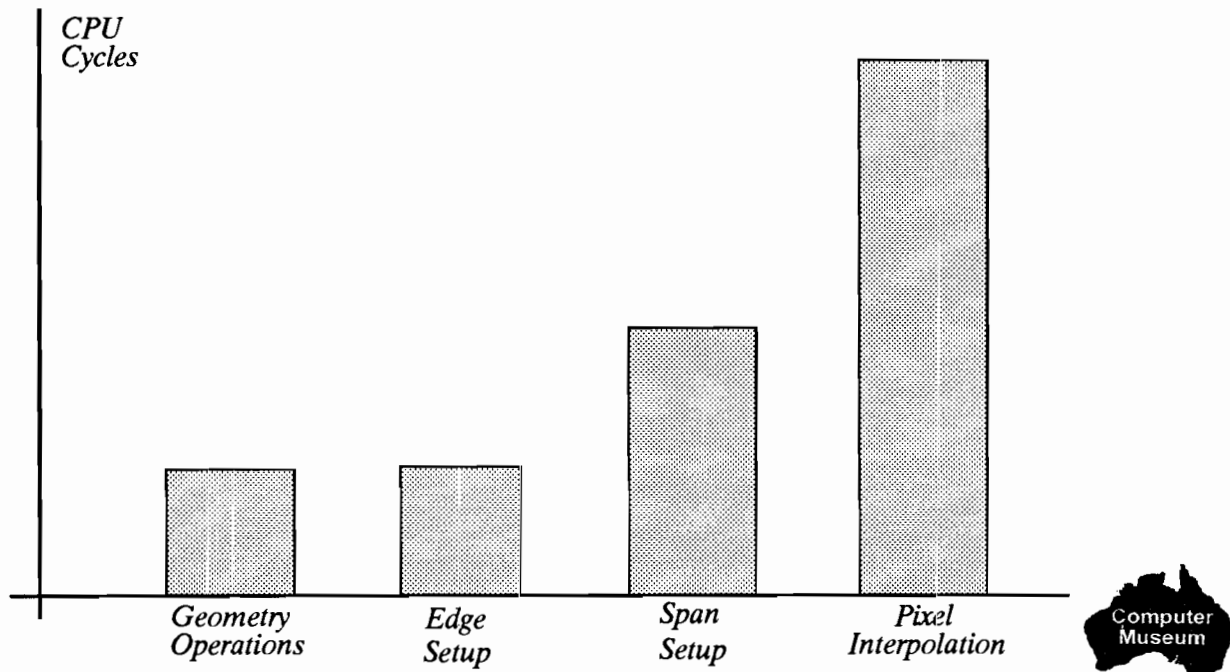


Figure 3. Relative CPU cycles required for each part of the pipeline

With this understanding, it is easy to envision a number of possible ways graphics hardware can be added to improve graphics performance. For ease of data transfer and for maximum performance impact, it is best to implement graphics acceleration beginning with pixel interpolation. Once that is accomplished, increasing amounts of hardware can be added until all graphics calculations are performed by graphics hardware. These possibilities can be grouped into the following categories:

- Maximum performance/maximum price: entire pipeline implemented in hardware.
- Optimized price/performance ratio: Geometry operations performed in the CPU.
- Inexpensive acceleration: Only pixel interpolation hardware.
- Minimum cost: Entire pipeline in software.

The remainder of this paper describes existing implementations by various workstation vendors of these architecture types.

FULLY-ACCELERATED PIPELINE (MAXIMUM PERFORMANCE POTENTIAL/MAXIMUM PRICE)

Most 3D graphics products today use an architecture based on the one needed for maximum performance, with the entire pipeline implemented with specialized graphics hardware. Such products include:

- DEC PXG Turbo
- Evans and Sutherland ESV systems

- IBM Gt4x
- Silicon Graphics Elan and VGX
- Silicon Graphics Reality Engine
- Sun GT

What is notable about these systems is that they all use special purpose floating–point acceleration for geometry operations and custom or semi–custom VLSI for rasterization (i.e., edge setup, span setup and pixel interpolation). There are three main approaches taken in the implementation of the geometry section of the pipeline:

1. An array of digital–signal processing (DSP) chips

One popular way to accelerate geometry operations is through the use of an array of DSP chips. Parallel arrays have the advantage that no single part of the geometry pipeline is the performance bottleneck, as is the case with serial arrays (unless load–balancing is used between the stages.) Serial arrays, on the other hand, have the advantage that each stage can be customized to best fit its specialized function. The Evans and Sutherland ESV systems and the IBM Gt4x both use an array of DSP chips to handle the floating–point requirements of geometry operations. E&S's two–dimensional array allows both parallelism in the processing of various primitives and parallelism of stages within the geometry pipeline. IBM's serial array is somewhat smaller and less powerful, but minimizes the bottlenecking problem by load–balancing the processors when load conditions change.

2. A single–instruction/multiple data (SIMD) arrangement

Silicon Graphics chose a SIMD approach (a common control section and multiple floating–point ALUs) with the VGX and Elan graphics subsystems so that multiple vertices of a polygon or a polyline can be processed at once. Since essentially the same computations are performed on each vertex, the duplication of control is avoided resulting in a cost savings. A main drawback is that the performance does not scale well when polygons with more than four vertices are processed and when additional computations are needed for operations such as clipping.

3. Embedded microprocessor(s) with fast floating–point capabilities

The Sun GT, the DEC PXG Turbo, and the Silicon Graphics Reality Engine all use the Intel i860 processor in their implementations. By employing a general–purpose processor with cache, a large amount of code space can be implemented with inexpensive DRAM, thereby providing the user with a somewhat richer accelerated feature set. Efficient parallelism can be obtained with multiple processors over a wide range of conditions because of their general–purpose nature. DEC's PXG Turbo and the Sun GT contain a single i860. At the highest reaches of graphics performance (and price) is the Silicon Graphics Reality Engine, which employs up to eight i860s for geometry operations and a whopping 180 ASICs for rasterization acceleration.

Hewlett–Packard was an early pioneer to use this type of architecture with the SRX in 1986, the TurboSRX in 1988, and the TurboVRX in 1990. At that time, a fully–accelerated pipeline was needed to deliver interactive performance.

Regardless of which of the three approaches are taken to implement a fully-accelerated pipeline, this type of architecture has a number of problems. First, since the entire pipeline is in hardware, the cost is relatively high. Second, graphics performance does not scale with CPU performance. That is, even as CPUs become much faster, graphics will see no improvement unless the graphics system itself is upgraded. Third, from an application viewpoint, since the geometry processors cannot access data directly in virtual memory without intervening control steps, large data bases cannot be handled effectively.

ACCELERATED RASTERIZATION (BEST PRICE/PERFORMANCE)

Recently, CPUs have reached a level of performance which enables them to perform part of the graphics pipeline in a system which exceeds the performance of most products with fully-accelerated pipelines. One such CPU is the PA-RISC 7100 processor used in HP Series 700 workstations [DeLano]. By allowing the CPU to perform the geometry part of the pipeline, the workstation does not incur the cost of specialized transform engines, making it far more affordable. (A PA-RISC 7100 CPU delivers approximately the same performance as the four i860s deliver in the TurboVRX T4.) Although a system like this one may not be as fast as *all* fully-accelerated systems at a given point in time, it strikes a good balance between the system cost, performance, and features.

There are other less obvious advantages to this type of architecture. For example, when the system CPU is upgraded, not only do ordinary compute-intensive operations speed up, but graphics commands go faster as well. Thus investment in graphics hardware is maintained. (See Figure 4 to show for how this applies to the CRX-24Z graphics subsystem.) A fully-accelerated graphics system will show very little or no such graphics performance increase. Another advantage of the accelerated rasterization architecture is that because the graphics software is resident in the virtual memory space of the processor, the graphics feature set is not constrained by the amount of code or data memory resident in the graphics hardware.

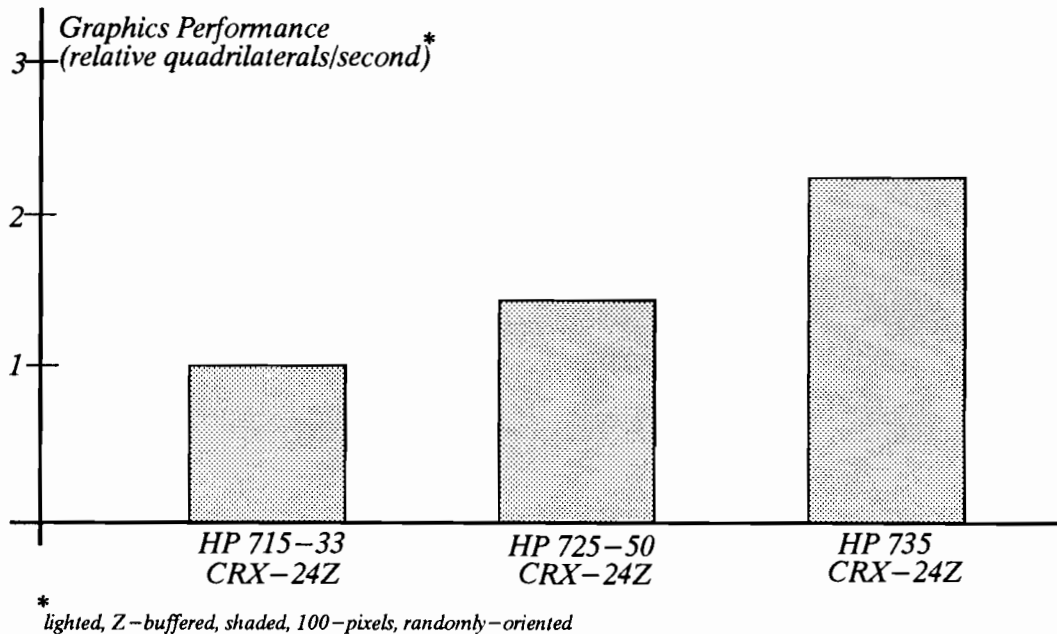


Figure 4. Relative Performance of CRX-24Z graphics with different host processors

While the concept of accelerated rasterization was applied earlier in “graphics supercomputers” such as the Stellar GS1000 [Apgar] and the Apollo DN10000VS [Kirk], the price of these systems were out of reach of the vast majority of users. The high price was due primarily to the cost of having multiple processors to achieve high performance. HP’s CRX-24Z attachment to the Series 700 workstations takes advantage of fast single-processor performance to make this architecture more affordable. A detailed description of the CRX-24Z design and architecture can be found in NCGA’s 1992 proceedings [Norrod 92].

The latest entry of this architecture type is the HP CRX-48Z. Like the CRX-24Z, it relies on the CPU for geometry operations, but has two to ten times the rasterization power and a second 24-plane image buffer. The CRX-48Z (built with an expanded configuration of the same VLSI rasterization components [Norrod 91] as the CRX-24Z) has enough rasterization performance to last well beyond the single-CPU PA-RISC 7100 products available today.

ACCELERATED PIXEL INTERPOLATION (INEXPENSIVE ACCELERATION)

By accelerating only the pixel interpolation part of the pipeline, significant graphics performance gains can be achieved while adding only a small amount of hardware expense [Horning, Dowdell]. To date, two products have been introduced with accelerated pixel interpolation: Silicon Graphics’ IRIS Indigo Entry Color (not to be confused with XS or Elan graphics) and HP’s CRX graphics family with PowerShade software.

Both the Indigo and the CRX-24/PowerShade have acceleration for pixel generation, but the two products have somewhat different amounts of acceleration. Indigo has a color interpolator in its graphics controller chip and relies strictly on CPU software to do Z buffer hidden-surface calculations [SGI]. Pass/fail information for several pixels is encoded into a single word and passed to the graphics controller.

HP's approach is to use the custom memory controller such as in the 735 and 755 products to accelerate pixel interpolation. Interpolated and Z-buffered pixels are sent from the memory controller to the CRX-24 (24 plane) frame buffer. The advantages of having the memory controller do pixel interpolation are two-fold: 1) the CPU can be performing the next span setup while pixels are being interpolated providing added graphics performance, and 2) Z data does not flush application data from the cache, thus preserving application performance.

SOFTWARE-ONLY PIPELINE (MINIMUM COST)

The lowest possible cost can be achieved if all graphics operations are performed in the CPU. 3D shaded graphics are implemented entirely in software, such as in HP's entry-level 715/725 Color systems with PowerShade. It is worth noting that its 3D quadrilateral performance is as fast as the maximum performance available on a workstation with a fully-accelerated pipeline just five years ago.

Below is a graph showing relative quadrilateral performance of selected HP workstation products, including one from each of the four basic architectures described in this paper. Compare this graph with Figure 3. Note the tremendous increases in graphics performance that can be achieved as more of the pipeline is implemented with special-purpose hardware. Also note that the amount of graphics acceleration can be chosen according to what best fits the user's needs and budget.

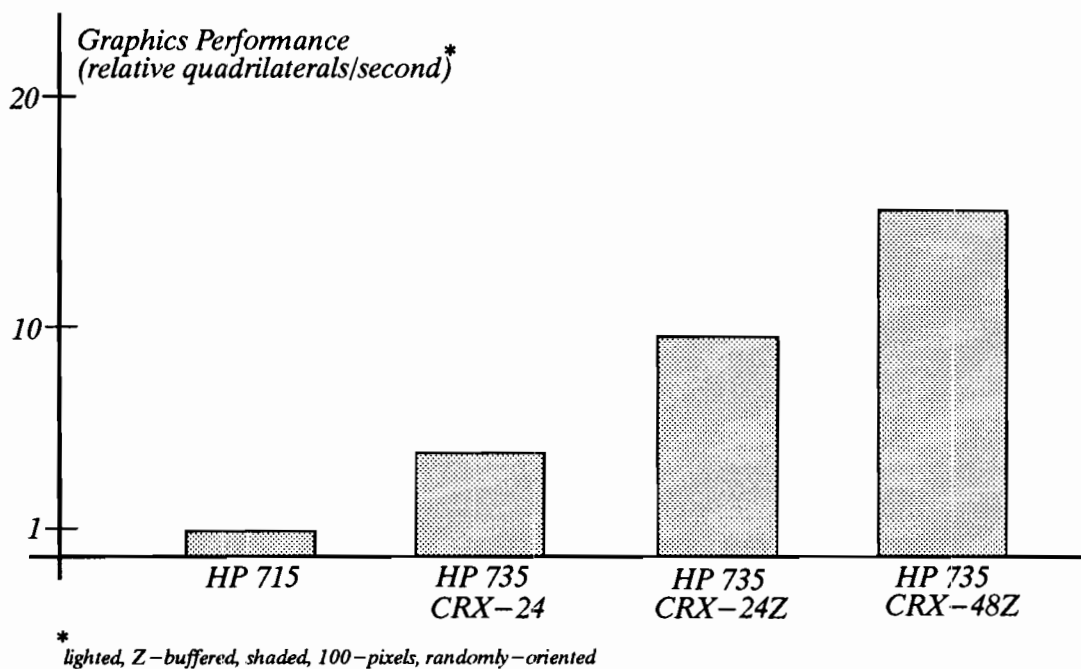


Figure 5. Graphics performance of various HP workstations

SYSTEM-LEVEL APPROACH TO GRAPHICS PERFORMANCE

Best system price/performance can be achieved if graphics needs are considered as part of the overall workstation system design, including the CPU instruction set, the graphics software architecture, the system software architecture, and the graphics

hardware. The HP Series 700 CPU was designed to improve the performance of all the above systems [Dowdell]. A number of features were added (including pixel interpolation in the memory controller) which add virtually no cost to the system, but which increase performance by as much as a factor of two. Another facet of the graphics system, graphics software, is designed so that any graphics program written for a Series 700 workstation and linked with shared libraries will run with any of the graphics systems listed above.

CONCLUSION

Current workstation vendors are improving their 3D graphics products by both refining existing architectures and developing new ones. These new architecture approaches not only better system price/performance, but also increase the number of options available to the user. Users can now choose from 3D products which span a factor of 15 in performance, as measured in 3D quadrilaterals per second. In order to achieve leadership graphics price/performance in the 1990s, workstation architectures must be designed from a system-level viewpoint based on a clear understanding of the graphics pipeline.

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Scalable Graphics Enhancements for PA-RISC Workstations

Casey Dowdell Larry Thayer
Hewlett Packard Company
3404 E. Harmony Road MS# 73
Fort Collins Colorado 80525

Abstract: *The addition of graphics specific features to the series 700 system architecture has improved graphics performance by 33% to 100% across various graphics workloads relative to the base system architecture. The model 735, which incorporates a 143 SPECmark PA-RISC CPU, is capable of rendering over 1,000,000 3D vectors per second and 30,000 independent shaded, z buffered quadrilaterals per second using a simple entry level frame buffer. Further improvements in performance may be obtained by partitioning the graphics pipeline between the CPU and dedicated rasterization and geometry accelerators.*

Enhancements to the CPU include polygon rasterization with virtual memory z buffer support, graphics specific floating-point, and graphics specific data path features.

1. Introduction

In many typical applications, the perceived system performance of a graphics workstation is defined as much by the display performance as it is by the computational performance. In order to achieve a sustainable price/performance advantage, HP has redefined the graphics system design task to be an integral element of the overall workstation system design task. HP's system level approach to graphics is focused on achieving high performance through improved efficiency, and lower cost through reduced redundancy.

From a product perspective, a system level approach to graphics means that the CPU, when configured with a simple frame buffer, is capable of providing excellent X windows and 2D/3D wireframe performance. Some of the markets which HP serves require 3D shaded graphics capabilities. This in turn requires that the same base system configuration be capable of providing useful 3D shaded graphics performance. In order to meet higher 3D shaded graphics performance requirements, accelerators have been developed which tap into the base level graphics drawing pipeline.

A brief description of each of the products described in this paper is given below.

The 715 and 725 are low cost workstations which incorporate an 8 bit color or gray scale frame buffer on the system mother board.

The 735 and 755 systems are more powerful workstations which may be configured with any of the following graphics options.

	CRX	CRX-24	CRX-24Z	CRX-48Z
Planes	16	32	32	56
Z Buffer	SW	SW	HW	HW
Config	Internal	Internal	Internal	External

Many unique features which specifically improve graphics display performance have been incorporated into the series 700 PA-RISC CPU. Current implementations of HP's X11, Starbase, and PEX graphics software libraries utilize the new processor feature set, and provide a common software interface to the range of graphics options. These libraries are available as runtime linkable modules, which may be used by applications without recompilation or relinking.

A CPU, which provides scalable graphics performance, must be able to accommodate a broad range of system requirements. The set of operations which must be performed, in order to convert a graphics library call into a screen image, is known as the graphics pipeline. One way to scale performance is to partition the graphics pipeline between what is implemented in the system CPU and what is implemented in specialized graphics hardware. Figures 1,2,4-6 represent several possible partitionings of the graphics pipeline.

Since data and computation expand in the latter stages of the graphics pipeline, performance can be improved most efficiently by adding hardware to the end of the pipeline. For the lowest cost system, the CPU must perform each element of the graphics pipeline, from display file storage to image storage. The performance can be improved by using special hardware for the various parts of the graphics pipeline, beginning with image storage and working up the pipeline. For example, nearly all computer graphics displays use a hardware frame buffer to store the image instead of main memory. The memory system has been relieved of this function with special hardware (a frame buffer), due to the prohibitive bandwidth requirements of image refresh. Further performance improvements can be

achieved by using special hardware for rasterization (setting the value of individual frame buffer locations) and by adding special geometry processors.

2. X11 performance

The outstanding X11 performance of the series 700 systems is based upon 6 system characteristics: well written code, a processor with state of the art integer and floating-point performance, fast data movement within virtual main memory, fast data movement between virtual main memory and the frame buffer, an effective processor interface to the frame buffer, and, of course, a fast frame buffer. Optimizing X11 performance requires that each of these elements be balanced, with no single element presenting a performance bottleneck.

All series 700 system frame buffers provide line and rectangle drawing support. X11 library calls which cannot directly take advantage of these functions are performed by the software. The graphics pipeline is thus partitioned before or after the rasterization stage, depending upon the operation being performed.

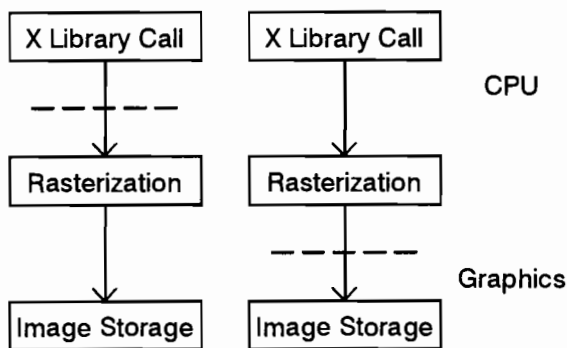


Fig 1. X Window Pipeline Model

3. 2D and 3D wireframe performance

Two dimensional (2D) and three dimensional (3D) wireframe application performance is most often characterized by vector rasterization rates, (wireframe refers to line drawings which represent 3D objects). Since cost is often a major consideration, these applications can be addressed by implementing the display file and the geometry processing in the CPU, with a simple vector rasterization engine in the graphics system. This is shown in figure 2. The 715/725 Color and 735/755 CRX models are implementations of this architecture.

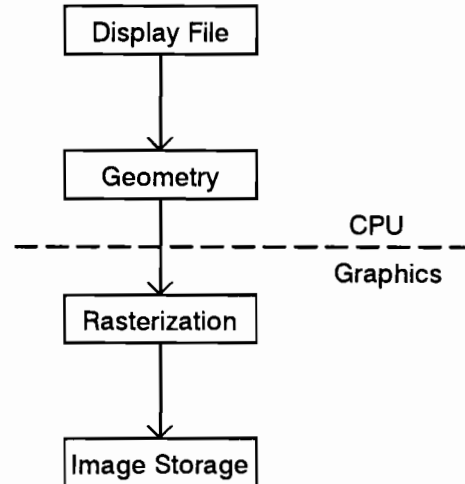


Fig 2. 2D and 3D Wireframe Pipeline Model

4. 3D shaded graphics performance

Solid objects are represented by a collection of shaded and z buffered polygons. The 3D shaded graphics pipeline can be thought of as comprising the five steps listed below. Figures 4-6 refer to step 1 as "display file", step 2 as "geometry", and steps 3,4 and 5 as "rasterization".

1. *Display file access* - The data which defines each polygon being drawn must be obtained from the application.

2. *Generation of screen coordinate vertices* - This step includes applying the appropriate transformations to the data which defines each polygon, applying the specified lighting to the polygon, and clipping the polygon to the window boundary. These operations tend to be very floating-point intensive.

3. *Polygon decomposition and edge setup* - Polygons need to be broken down into simpler components and the edge slopes determined so the polygons can be rasterized. Here, both floating-point and integer operations are needed.

4. *Edge intersection and span setup* - Once the edge characteristics have been determined, the intersections of the edges with the individual horizontal spans which make up the polygon must be computed.

5. *Pixel generation* - This step includes performing the color interpolation and Z buffering of the individual pixels along a particular horizontal span.

Note that since there are typically several spans per pair of edges, the required computation is greater for step four than for steps one through three. Similarly, there are typically several pixels per span, so the computational require-

ments of pixel generation within the span are even greater.

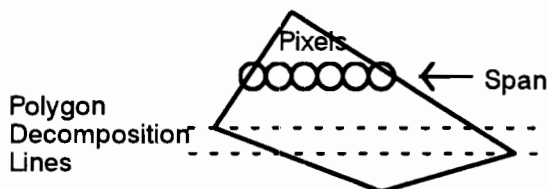


Fig 3. Polygon Rasterization

Performance is improved when using a span interpolator to assist the software by performing step 5. This improves the overall 3D shaded graphics performance by about a factor of 2. The 735/755 CRX and CRX-24 implement this architecture.

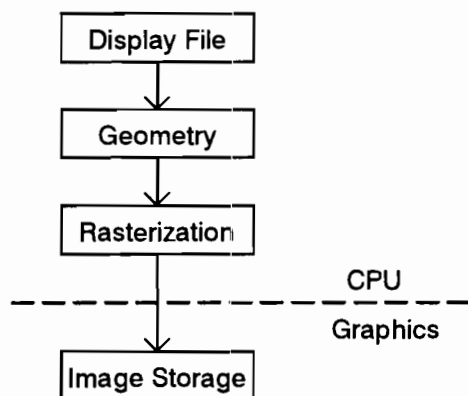


Fig 4. Low-end 3D Shaded Graphics Pipeline

Another factor of 3 or 4 in 3D shaded graphics performance is achieved by adding dedicated hardware to perform steps 3, 4, and 5 of the pipeline as in figure 5. This architecture is represented by the 735/755 CRX-24Z and by the 735/755 CRX-48Z.

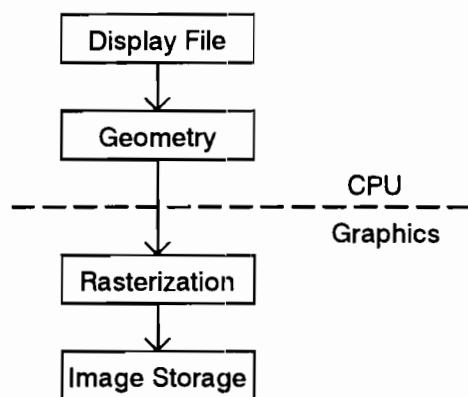


Fig 5. High-end 3D Shaded Graphics Pipeline

5. New Features

5.1. The system I/O bus

The series 700 system I/O bus is designed to meet the specific needs of graphics display controllers, which are markedly different from the needs of disk or network controllers. X11 performance in particular is dependent upon high speed random access to the frame buffer. Many I/O busses, such as SBUS and Turbochannel, provide good burst performance but relatively poor random access performance. For example, the SBUS is limited to 33 mb/sec during random access sequences. [1] The series 700 system I/O bus is a non-multiplexed address/data bus which supports data transfer rates of 132mb/sec during random access sequences.

5.2. Data transfers between virtual memory and the frame buffer

The most direct way of performing such data transfers is to move the data under program control through the use of load and store instructions. In addition to the inherent simplicity, there are several other benefits which this method provides. The virtual address to physical address translation is transparent to the software. Cache coherency is maintained in a software transparent manner since data is first moved from memory to the cache, and then subsequently moved from the cache to the system I/O bus. The entire data transfer process is defined by user-level software, so that calls to the operating system or driver code are not required. Finally, the system data paths are accessed on a word rather than block basis so that other transfers are not held off for long periods of time.

Unfortunately, the frame buffer bandwidth requirements cannot be met by using simple programmed I/O. Also, moving large amounts of graphics data through the data cache degrades system performance by displacing large amounts of application data from the cache.

In order to overcome these limitations, an instruction (Move32) was added to the CPU which moves a 32 byte block of data between main memory and the 32 bit system I/O bus. The Move32 instruction performs a translation between a specified virtual address and a corresponding physical address. The translation uses the processor's TLB, with standard exception handling and protection mechanisms operative. The physical address is then forwarded to the memory controller section which then begins the 32 byte transfer. If a processor data cache line contains data which represents the affected data in main memory, the cache line is flushed to main memory on writes to the system I/O bus, and is invalidated on reads.

The software developer thus has an instruction which improves data transfer rates by a factor of two (60 vs 30 mb/sec), retains all of the advantages of the method described above, including the simplicity, and because data is not

moved through the processor data cache, application data is not displaced.

5. 3. User visible cache prefetch

Moving large blocks of data directly using the memory controller is an effective means of providing image data to the frame buffer or display file data to a 3D geometry pipeline. However, system configurations which require the CPU to perform arithmetic processing of display file data must move data from the virtual memory system into the CPU register file. The process of accessing large display files from virtual memory for processing by the CPU is unique in several ways. Typical display files are larger than most system caches, while at the same time the data within the display file is typically used just once. Given this set of characteristics, the system cache is only usable in very localized cases (such as reusing vertices in a triangle strip definition). In modern processors, cache miss penalties can be high due to increasingly high processor clock rates. Reducing the number of data cache misses complements any improvements made in the arithmetic processing capabilities of the CPU. As the processing overhead is reduced, the data access overhead becomes a larger percentage of the total execution time.

Display file access patterns are often sequential or are otherwise easy to predict by the software. If the software could indicate to the processor that it will be requiring a particular data set to be present in cache soon, cache miss penalties would be reduced dramatically. An instruction (fetch32) was created to do that by requesting the memory controller to fetch 32 bytes at a specified virtual address and place them in the data cache. While the data is being fetched, the processor is free to continue executing instructions. If no attempt is made to access the specified data before it has been placed in cache then no cache miss penalty is incurred.

5. 4. Shading and Z buffering inner loop support

One of the goals of the project was to approximate the polygon rendering performance of an entry-level 3D system using only an inexpensive frame buffer. This meant that the CPU would have to implement the entire graphics pipeline, including polygon scan conversion.

Several new CPU instructions were considered, [2] but ultimately it was determined that the CPU execution unit by itself could not provide the parallelism required to significantly improve scan conversion performance. Instead, it was decided that the memory controller section would be enhanced to provide the inner loop processing across an entire horizontal span, leaving the CPU execution unit free to perform the edge stepping and span setup process.

Moving the inner loop processing into the memory controller hardware allows RGB and Z interpolation, as well as data formatting, to be performed in parallel. The memory access method was built on top of the Move32

instruction hardware. The memory controller reads 32 bytes from main memory into an internal buffer. The contents of the internal buffer are then compared with the interpolated Z values, modified appropriately, and are written back to main memory. In parallel with the Z processing, RGB values are interpolated across the span and are conditionally written to the graphics system over the 32-bit system I/O bus. Data cache thrashing due to Z buffer access is eliminated, since the Z buffer data is never moved through the cache.

Mapping the Z buffer into the virtual memory space of the CPU eliminates the need to allocate a section of physical memory at boot time, and allows the Z buffer memory to be used for other purposes when the Z buffer is not in use. In order to accomplish this, and to control the span processing hardware, a new interpolate instruction (Interpolate32) was created which behaves very much like the Move32 instruction. Both the virtual to physical address translation as well as the cache coherency check are performed just as described for the Move32 instruction. The physical address is then forwarded to the memory controller section. Each issuance of the instruction causes sixteen pixels to be rendered. Using the Interpolate32 instruction, pixels can be interpolated and Z buffered at a rate of 17 million per second.

The incorporation of polygon rasterization support in the PA-RISC CPU allows even the most inexpensive system configurations to provide interactive 3D shaded graphics performance. The cost impact is much less than 1% of the system cost. Only a few adders and some registers were added to a VLSI device whose dimensions were determined by the pinout, not by the amount of internal circuitry.

5. 5. Expanding the floating-point register file size

The floating-point register file which had been used in previous generations of the CPU consisted of 12 double precision registers and 4 floating-point status registers. It had been determined that the floating-point register file would be extended to include 28 double precision registers. Because most graphics software requires only single precision, it was determined that each double precision register would be split and defined as two unique single precision registers, for a total of 56 single precision registers. Several important inner loops within the graphics software are executed with their data sets entirely contained in the register file.

5. 6. The five operand instruction form

The floating-point section consists of a floating-point multiplier and a floating-point ALU. In order to support the parallelism between the two sections, a five-operand instruction form was developed which defines two source registers and one destination register for the multiplier section, and one source register and one source-destination register for the ALU section. The parallel execution sections as well as the five-operand instruction form fit well

with the floating-point requirements of many graphics routines.

5. 7. Clip test support

Clip testing is an operation performed on every polygon vertex to determine if the complete polygon is either entirely inside or outside the viewing window. The graphics clip check calculation requires a series of 6 compares followed by several logical operations used to develop an outcode bitfield. In order to improve the speed of this operation, the resulting sign bits of the sequential compares are accumulated in a dedicated condition register by the hardware. Branch conditions which indicate whether a polygon is entirely in or out of the window are formulated based on the contents of the condition register.

5. 8. Parallel divide and Square Root

The floating-point divide and square root section is implemented such that the floating-point MPY and ALU units are free to perform other useful work. In the hand coded portions of the graphics software, the floating-point MPY and ALU units are almost always kept busy during divide and square root operations.

5. 9. Integer multiply

In order to support 2D applications which transform 32 bit integer coordinates, a fast 32 bit integer multiplier was added to the floating point unit. The multiplier provides a full 64 bit result, which is required in order to maintain the entire dynamic range of results.

6. Performance analysis

In combination, the graphics enhancements provide a significant improvement in the performance of the application types discussed earlier. Figures 7-9 show how these enhancements improve the performance of each application type, using a 99 MHz, 143 SPECmark PA-RISC CPU. The bar graphs show the absolute performance achieved, while the pie charts show how each enhancement contributed to the overall improvement.

6. 1. 3D wireframe

The 735/755 CRX is a 3D wire frame system. An analysis of the 3D vector operation shows how the CPU enhancements have affected this operation. Display file reads are

improved by removing the cache miss penalty. The clip check, parallel multiply and add, and parallel divide enhancements each provide large percentage improvements as well. As shown in fig 7, the reduced CPU cycle counts correspond to a 100% improvement in 3D vector performance, moving from an original 580,000 vectors/second to well over 1,000,000.

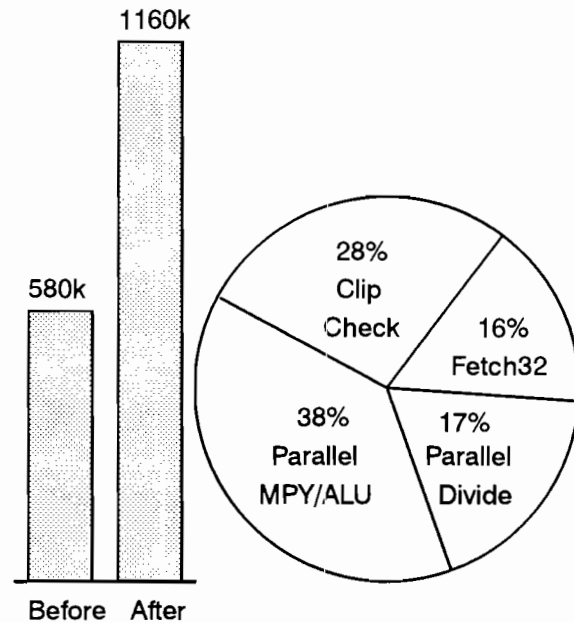


Fig 7. 3D wireframe vectors/sec

6. 2. Low-end 3D shaded graphics (quadrilaterals)

The 735/755 CRX-24 is a system which supports low-end 3D shaded graphics. When using an inexpensive frame buffer to draw independent, lighted, Z-buffered, shaded quadrilaterals, the graphics pipeline must be implemented entirely within the CPU. Fig 8 shows that the dominant savings is due to the color interpolation and Z comparing capabilities of the memory controller. The remaining cycles which are saved result from the various floating-point enhancements. The set of CPU enhancements allow the CPU to draw 30,000 independent, light-sourced, Z-buffered, 100-pixel quadrilaterals/second. This represents a 65%

improvement over the 18,000 which could have been achieved without the system enhancements.

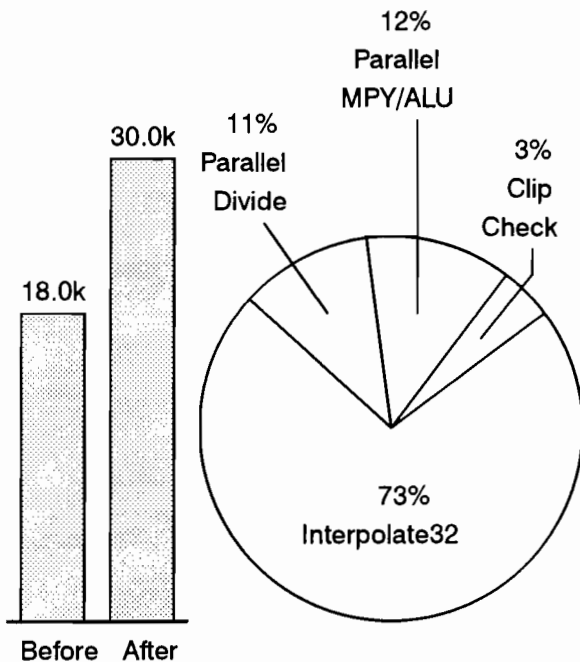


Fig 8. Low-end 3D Shaded Quadrilaterals/sec

6. 3. High-end 3D shaded graphics (quadrilaterals)

The 735/755 CRX-48Z, which is a high-end system, provides a polygon scan converter in order to relieve the

CPU of the rasterization task. An analysis, of the same 100 pixel quadrilateral case as above shows that the floating-point enhancements now play a much more significant role. As shown in fig 9, they combine to improve the performance by 33%, pushing the original 112,000 quadrilaterals/second to over 150,000.

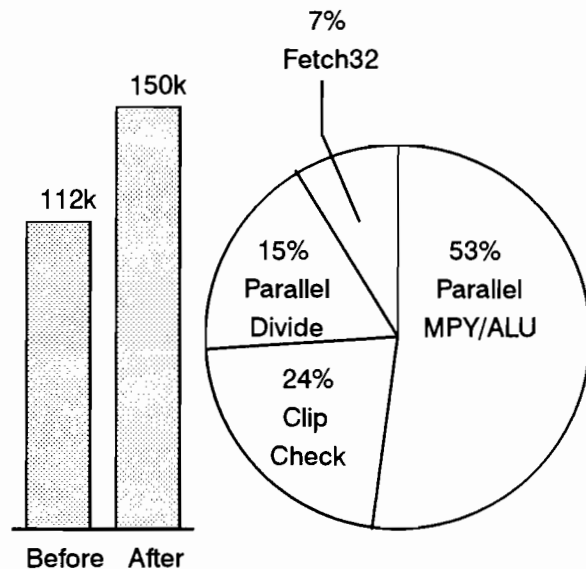


Fig 9. High-end 3D Shaded Quadrilaterals/sec

7. Conclusion

By taking a system level approach to the graphics system design, a workstation's graphics performance can be increased significantly with only a minimal increase in total system cost. In the three cases examined, the performance improvement ranged from 33% to 100%, while the overall system cost impact was much less than 1%.

New floating-point features include parallel floating-point multiplier and alu sections, "zero cycle" divides for perspective transformations and edge set up, "zero cycle" square root for lighting calculations, clip-check branch conditions, and a larger register file which allow many inner loops to execute with their data sets contained entirely in the register file. An instruction which moves data directly between virtual memory and the frame buffer is used to improve the performance of windows, animation sequencing, and high end 3D graphics. An instruction, which sup-

ports a virtual memory z buffer and color interpolation, was added in order to provide useful 3D shaded graphics performance in an entry level system. Cache miss penalties incurred during display list accesses are reduced through the addition of a non-stalling cache line prefetch instruction.

This paper documents how system price and performance benefit when system designers look beyond the simple integration of components and deliver a wholly conceived workstation design.

References

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2. Kohn, L., Margulis, N., "Introducing the Intel i860 64-Bit Microprocessor," IEEE MICRO; August, 1989

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United States:

Hewlett-Packard Company
4 Choke Cherry Road
Rockville, MD 20850
(301) 670 4300

Hewlett-Packard Company
5201 Tollview Drive
Rolling Meadows, IL 60008
(708) 255 9800

Hewlett-Packard Company
5161 Lankershim Blvd.
North Hollywood, CA 91601
(818) 505 5600

Hewlett-Packard Company
2015 South Park Place
Atlanta, GA 30339
(404) 955 1500

Hewlett-Packard Company
300 Apollo Drive
Chelmsford, MA 01824
(508) 256 6600
FAX: (508) 256 2384

Canada:

Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive
Mississauga, Ontario L4V 1M8
Canada
(416) 678 9430

Latin America:

Hewlett-Packard
Latin America Region Headquarters
Monte Pelvoux No. 111-2nd Floor
Lomas de Chapultepec
11000 Mexico, D.F.
(525) 202 0155

Japan:

Yokogawa-Hewlett-Packard Ltd.
Kohrakuen Shinjuku Bld.
15-7, Nishi Shinjuku 4 Chome
Shinjuku-ku, Tokyo 160
Japan
+81 3/5371 1351

Asia Pacific:

Hewlett-Packard Asia Pacific Ltd.
22/F Bond Centre
West Tower
89 Queensway, Central
Hong Kong
+852/ 848 7777

Australia/New Zealand:

Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Melbourne, Australia
+61 3/272 2895

European Headquarters:

Hewlett-Packard S.A.
Route du Nant-d'Avril 150
CH-1217 Meyrin 2/Geneva
Switzerland
+41/22/780 8111

Austria:

Tel: +43/222/2500 0

Belgium:

Tel: +32/2/761 3400

Czechoslovakia:

Tel: +42/2/471 73 21

Denmark:

Tel: +45/45/99 10 00

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