

HP 3000 Series 960 System

Technical data

HP 3000 Computer Systems

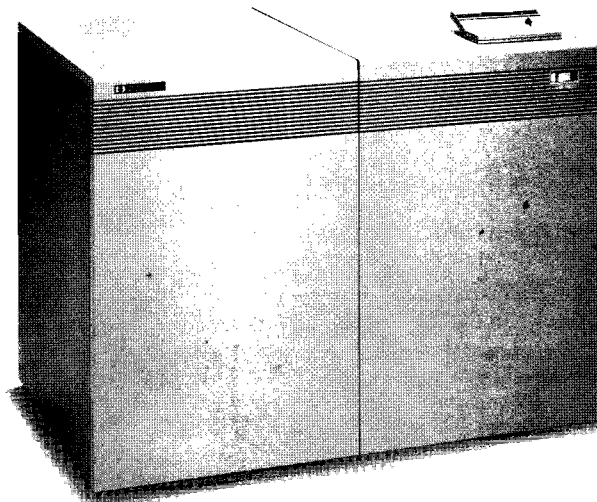
The HP 3000 Series 960 system is a high performance member of the broad family of compatible HP 3000 business computers. The Series 960 couples a high performance implementation of RISC-based HP Precision Architecture (HP-PA) with the MPE XL Operating System, which is optimized for commercial data processing and Online Transaction Processing (OLTP). This coupling of an OLTP-focused operating system and high performance RISC technology makes the Series 960 a reliable, cost-effective system for large-scale applications supporting several hundred online users. The Series 960 also uses an advanced implementation of Hewlett-Packard's proprietary NMOS III VLSI technology and is comprised of an impressively few number of parts, including a single-board processor. A convenient field upgrade to the high performance HP 3000 Series 950 and Series 955 systems, the Series 960 delivers incremental growth with a modular approach to extending the HP 3000 family. The Series 960 also utilizes its powerfully designed processor and a high performance floating point coprocessor to excel in compute-intensive applications. In total, the Series 960 provides

exceptional performance and functionality in multi-user, multi-tasking interactive and batch environments and runs a wide variety of financial, manufacturing, service industry and information management software to meet your data management needs

Features

- 15 MIPS CPU Performance
- Single-chip VLSI CPU, single-board processor
- 37 nanosecond system clock cycle
- 48 bit virtual addressing
- 128 Mbyte main memory standard, expandable to 256 Mbytes
- 512 Kbyte high-speed CPU instruction cache
- 512 Kbyte high-speed CPU data cache
- Ultra high-performance floating point coprocessor standard
- Advanced five-stage instruction pipelining
- 16K-entry Translation Lookaside Buffer
- Battery backup, auto restart standard
- Three-level I/O hierarchy providing high I/O bandwidth
- High-speed, 100 Mbytes/second System Memory Bus
- IEEE 802.3 standard local area network terminal connection
- MPE XL operating system
- Network and relational database management systems standard

HP 3000 Series 960 system



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Advanced technologies

HP Precision Architecture

The HP 3000 Series 960 system uses HP Precision Architecture (HP-PA) and a very powerful implementation of HP's proprietary NMOS III VLSI technology to produce a high performance, highly reliable system at a low cost. HP-PA builds on reduced instruction set computing (RISC), a design approach that delivers greatly simplified computers that are optimized to provide the highest performance for a given integrated circuit (IC) technology. In addition, the inherent simplicity of HP-PA means lower cost and higher reliability due to the need for fewer components.

The core of HP-PA is an instruction set containing 140 carefully selected, fixed-format instructions. Because the instruction set is simple, instructions can be hardwired directly in the central processing unit (CPU), eliminating the need for microcode and the necessity to decode complex instructions.

HP-PA utilizes a Load/Store design to reduce the number of relatively slow memory accesses, as most operations are performed register-to-register. To further enhance performance, optimizing compilers are used to schedule instructions and manage the instruction pipeline. With hardwired control, a Load/Store design, and optimizing compilers, one instruction is executed with virtually every clock cycle. Single-cycle execution provides much of the performance benefit of HP-PA over traditional architectures.

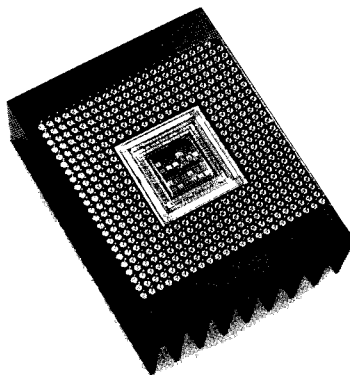
HP-PA goes beyond RISC to incorporate other features that greatly enhance its performance and functionality. For example:

- Support for coprocessors (i.e., floating point)
- Extended addressing
- Memory-mapped I/O subsystem

VLSI technology

The HP 3000 Series 960 system is implemented using a powerful design in HP's proprietary NMOS III VLSI technology, allowing the entire Series 960 CPU to be put on a single 1.4cm die, comprising 180,000 transistors and packaged in a 408-pin pin-grid-array (PGA). This 408-pin PGA allows separate paths for data and instructions from the cache to memory and enables single-cycle execution for every 37 nanosecond clock cycle. Furthermore, the entire processor, including a 1 Mbyte cache, 16K-entry Translation Lookaside

Single-chip VLSI CPU



Buffer (TLB), and the high performance floating point coprocessor, exist on a single printed circuit board.

System organization

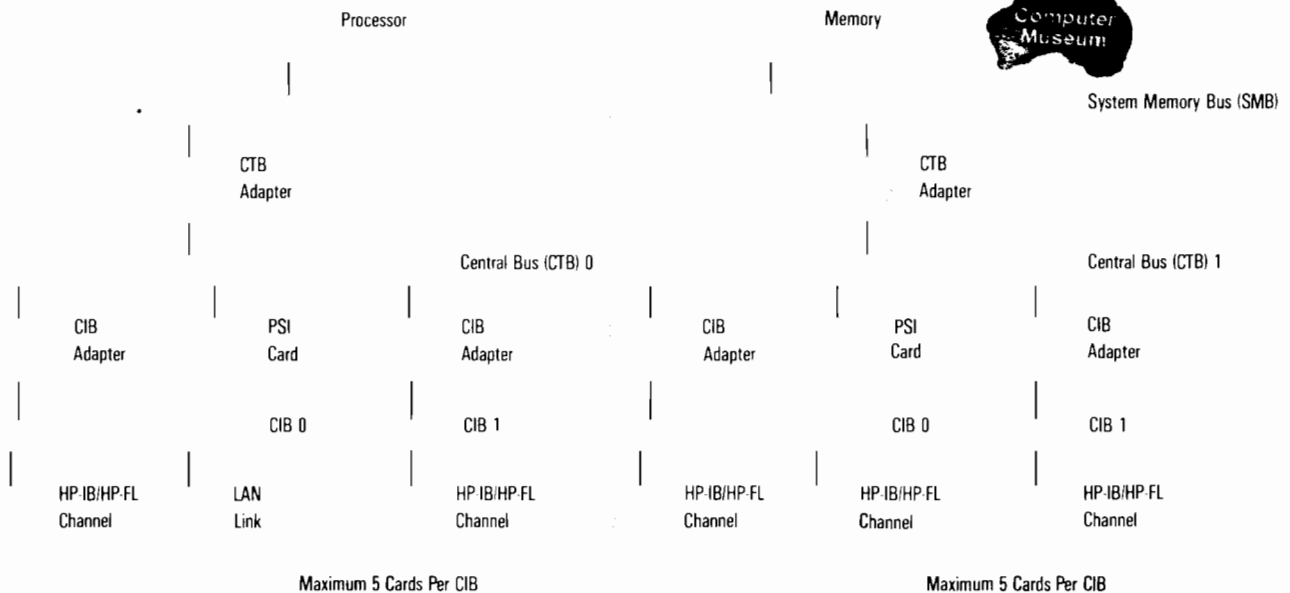
The processor communicates with main memory via the System Memory Bus (SMB). The SMB is a very high-speed bus that provides a 64-bit data path and can support sustained data transfer rates of up to 100 Mbytes/second. The SMB connects to two Central Buses (CTBs) through separate CTB adapters. Each CTB supports two channel I/O buses (CIBs) via separate CIB adapters. The CIBs support I/O interfaces to peripheral devices and Local Area Network (LAN) links.

The CTBs also support Programmable Serial Interfaces (PSI cards), allowing the HP 3000 900 Series systems to be linked to other computers in a distributed processing environment. The HP 3000 Series 960 system supports 8 PSI cards.

The entire HP 3000 Series 960 system processor (implemented using HP's proprietary NMOS III VLSI technology), the 1 Mbyte cache for data and instruction, and the 16K-entry Translation Lookaside Buffer reside on a single printed circuit board. The design includes a Central Processing Unit (CPU), a Translation Lookaside Buffer Control Unit (TCU), an Instruction Cache Control Unit (ICCU), a Data Cache

Instruction pipelining

is fetched from cache. The specified instruction is decoded during the second stage, and the resulting CPU internal calculation or function is performed during the third stage. The fourth stage is used to generate the condition code for the corresponding result. Finally in the fifth stage, a general purpose register is set with the corresponding cache or internal result. Excepting penalties for cache misses, etc., the net effect is that one instruction completes with every 37 nanosecond CPU cycle.

[illegible]

Caches

The cache is a high-speed buffer for the CPU that minimizes the number of relatively slow transactions with main memory. The HP 3000 Series 960 system uses a 512 Kbyte high-speed CPU instruction cache and a 512 Kbyte high-speed CPU data cache. Each cache uses a *write-to* management scheme, is two-way associative (direct mapped), and is organized in sets of 16,384 cache lines, having 32 bytes per line. Data modified in the cache is written to main memory only when the processor requires other data to be in that cache location, or when a direct memory access (DMA) operation is performed within that data area, or upon a power fail.

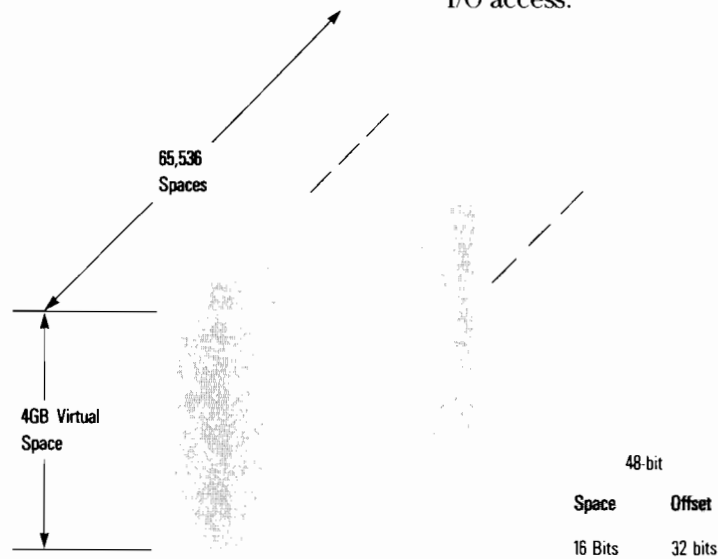
Floating point coprocessor

Single-precision and double-precision floating calculations are performed by the floating point coprocessor. The coprocessor is designed using ultra high-performance chips and significantly decreases the time required to perform floating point calculations. The floating point coprocessor and the CPU can operate in parallel, allowing for increased performance in applications that use floating point.

Virtual memory management

Virtual addresses on the Series 960 are 48 bits in length. This greatly extended address space ensures sufficient expandability to meet evolving software needs. Virtual memory is divided into a set of 65,536 spaces, with each space 4 Gbytes in length. Spaces are further divided into fixed-length, 2 Kbyte pages, with a given page holding either data, code, or both. A single data structure can be up to either 1 Gbyte or 4 Gbytes in length (compiler dependent), and code can span multiple spaces.

Figure 3. Virtual Address Space



Virtual address translation

Virtual-to-physical address translation is done by Translation Lookaside Buffers (TLBs) that cache recently accessed virtual page translations and convert the 48-bit virtual address into a 30-bit physical address. The Series 960 TLB holds translations for 16,384 virtual pages, and is split into an 8,192-entry instruction TLB and an 8,192-entry data TLB. Page-level access protection is provided on the Series 960, and the TLB hardware supports protection mechanisms to ensure that the currently executing process has sufficient authorization to perform the requested data, code, or I/O access.

Memory subsystem

The HP 3000 Series 960 system supports 128 Mbyte of main memory standard and is expandable to 256 Mbytes in 16 Mbyte increments. The memory subsystem uses 1 Mbit, nibble-mode dynamic RAMs. Main memory has battery backup to ensure that information is maintained for a minimum of 15 minutes in the event of an interruption in AC power. This allows the operating system to be automatically restarted and processing to continue without data loss upon resumption of power.

The internal memory word size is 72 bits, with 64 data bits of two 32-bit words, plus 8 bits for error detection and correction. Single-bit memory errors are automatically corrected, with automatic detection of all double-bit errors.

I/O subsystem

I/O buses

Channel I/O Buses (CIBs) support up to five cards each for interfacing peripheral devices and

providing for local area networking. Each CIB adapter provides DMA functions and has a data throughput capacity of up to 5 Mbytes/second. Two CIB adapters directly connect to each Central Bus (CTB). Each of the two CTBs run synchronously with a 9-MHz clock and can support data transfer rates of up to 20 Mbytes/second.

Memory-mapped I/O

Input/output operations are initiated and controlled via a memory-mapped I/O scheme, such that the processor only needs to access reserved virtual or physical memory locations to control I/O operations. Memory-mapped I/O allows for streamlined I/O operations and thus increases system performance in I/O-intensive applications.

Peripheral connection

Disks are connected via HP Fiber-Optic Link Interfaces (HP-FL), each supporting up to 8 disks. Each HP-FL can support a data transfer rate of up to 5 Mbytes/second. Tapes and printers (as well as disks) are

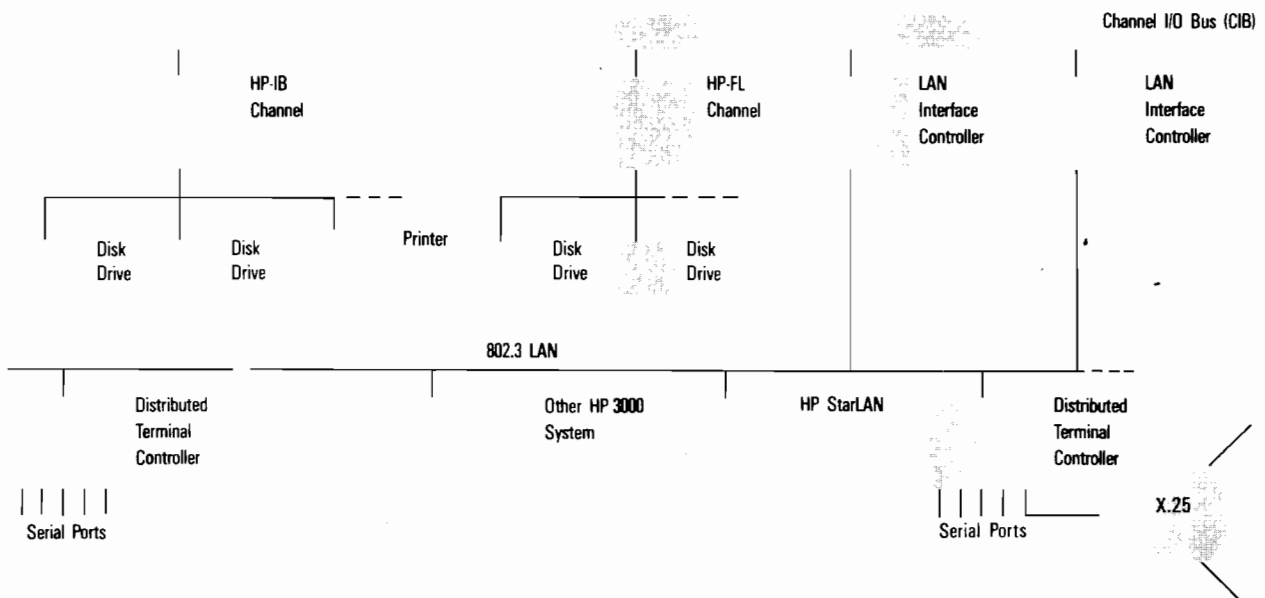
connected via the 8-bit wide, IEEE-488 standard Hewlett-Packard Interface Bus (HP-IB).

Workstation and serial printer connection

Connections for workstations, serial printers, and other serial devices are provided via Distributed Terminal Controllers (DTCs) that are distributed over an IEEE 802.3 standard local area network (LAN). This flexible connection scheme allows DTCs to be situated in the department that they service, saving the cost and effort of running cables from each workstation back to the processor. A workstation connected via a DTC can switch between HP 3000 Series 900 systems connected over the same LAN. Each DTC can support up to 48 direct connect ports, or 36 modem ports, or a combination of the two. Both RS-232C and RS-422C interfaces are supported.

PCs can also be connected to the 802.3 LAN via HP StarLAN which is a local area networking scheme using unshielded twisted pair (or phonewire).

Figure 4. Peripheral Connection



Environmental specifications**AC Input Voltage**

208 VAC, three phase @ 60 Hz
380 VAC, three phase @ 50 Hz
415 VAC, three phase @ 50 Hz

Input Voltage Tolerance

± 10%

Input Voltage Frequency

50 Hz or 60 Hz (± 2%)

Input Current

8.0 amps @ 208 VAC 60 Hz
4.4 amps @ 380 VAC 50 Hz
4.0 amps @ 415 VAC 50 Hz

**Input Power Consumption,
Maximum**

2,300 watts

Heat Dissipation, Maximum

7,900 BTU/hour

Physical Dimensions

Height: 1.00 meter (39 inches)
Width: 1.30 meters (51 inches)
Depth: 0.71 meters (28 inches)

Weight

400 Kg (880 lbs)

Operating Temperature, System

20–25.5 degrees C
(68–78 degrees F)

**Relative Humidity, System
(Operating)**

40–60% (noncondensing)

Altitude (Operating)

Up to 15,000 feet

**Battery Backup Time,
Minimum**

15 minutes

Acoustics

73 dB (A) Sound Power

Regulatory Compliance**Safety**

UL Listed (UL 478), CSA
Certified (C22.2 No. 220)
Compliant to IEC 380/435

Electromagnetic Interference

Complies with FCC Rules,
Part 15, Subpart J for Class A
computing device. FTZ 1046
General Permit (Manufacturer's
Declaration) VCCI Class 1

**System-to-system
datacommunications**

HP NS3000 XL Network Services provides virtual terminal, network file transfer, remote file and database access, network interprocess communication, remote process management between HP 3000s on an IEEE 802.3 LAN using HP LAN Link/XL, or over wide areas using the HP DTC X.25 XL Network Link or the HP NS Point-to-Point Link. HP SNA IMF, HP SNA NRJE, and HP SNA LINK provide HP 3000-to-IBM system communications.

System software

Listed below are software products currently available for the HP 3000 Series 960 system as of MPE XL Release 2.0. This list will be expanded over time as development and testing of additional software products continue. Check with your local sales representative for more information.

Application software

A wide range of solutions is available for the HP 3000 systems in application areas that include manufacturing, financial management, and information management. Your sales representative can provide more information that is specific to your needs.

Table 1. System Software

Operating System	Datacommunications	Utilities
MPE XL	HP NS3000/XL HP LAN Link/XL NS Point-to-Point 3000/XL HP SNA IMF HP SNA NRJE HP SNA Link HP DTC X.25 Network Link DTC Terminal Access NS LAN Gateway Openview DTC Manager SNA DHCF/XL BSC Remote Job Entry/XL BSC Link/XL LU 6.2 API/XL	FCOPY/XL SORT-MERGE/XL Mirrored Disk/XL* TurboSTORE/XL LaserRX/MPE HP GLANCE Native Mode Spooler* NLIO*

*Available with MPE XL Release 2.1.

Office Automation	Languages	Information Management
Business System Plus: - HP DeskManager - HP Information Access Cooperative Services HP AdvancePrint HP AdvanceLink HP Schedule HP ListKeeper TDP HP Spell	COBOL II/V COBOL II/XL Pascal/V HP Pascal/XL FORTRAN 66/V HP FORTRAN 77/V HP FORTRAN 77/XL HP Business BASIC/V HP Business BASIC/XL BASIC/V SPL/V RPG/V HP C/XL Transact/XL HP RPG/XL	TurboIMAGE/XL TurboIMAGE DBchange/V ALLBASE/SQL ALLBASE/4GL ALLBASE/NET ALLBASE/QUERY Inform/V Report/V HP Toolset/XL Information Access/XL KSAM/V Dictionary/V HP System Dictionary/XL BRW/V BRW/XL HP Edit

Ordering information

The HP 3000 Series 960 SPU includes 128 Mbyte main memory, two CIBs, one LAN interface, a console connection, and two HP-IB channels. Return credits are available when upgrading HP 3000 systems other than the Series 955 or Series 950 to the Series 960. The Series 960 is also available as a field upgrade from the Series 950 or Series 955 system. For more information, contact your local HP sales office.

Product Number	Description
A1130A	HP 3000 Series 960 SPU Preconfigured System. Includes SPU with 128 Mbyte Memory, two CIBs, two HP-IB Channels, one LAN interface, MPE XL Fundamental Operating Software, ALLBASE/XL Database Management System, and System Dictionary/XL.
A1136A	HP 3000 Series 960 SPU hardware. Includes SPU with 128 Mbyte Memory, two CIBs, two HP-IB Channels, one LAN interface. Includes no Software.
A1133A	HP 3000 Series 955 to Series 960 Field Upgrade. Includes 32 Mbyte Memory.
A1132A	HP 3000 Series 950 to Series 960 Field Upgrade. Includes 64 Mbyte Memory.

Supported peripherals

Listed here are peripheral devices currently available for the HP 3000 Series 960 system as of MPE XL Release 2.0. This list will be expanded over time as development and testing of additional peripherals continue. Check with your sales representative for more information.

Table 2. Supported peripherals

Terminals	Disk Drives	Tape Drives	Printers
2392A	7937H/XP	7978A/B	2680
2393A	7933H/XP	7974A	2687
2397A	7935H/XP	7979A	2688
2394A	7936H/XP	7980A	2566A/B
2622A	7937FL	7980XC	2565A
2623A			2686
2624B			2933
2625A			2934
2627A			2562C
2628A			2563A/B
3081A			2564B
3082A/B			2567B
700/92			LaserJet 2000
700/94			LaserJet
HP Vectra CS/ES/RS PCs			LaserJet II/IIiD
Portable Plus			C1202A
Touchscreen PC			C1200A

Support services

A wide range of hardware and software support services are available worldwide for all HP 3000 products. Contact your HP sales representative for details on available support services.

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