

HEWLETT-PACKARD

Series 935

HP 3000 Computer Systems

Data Sheet

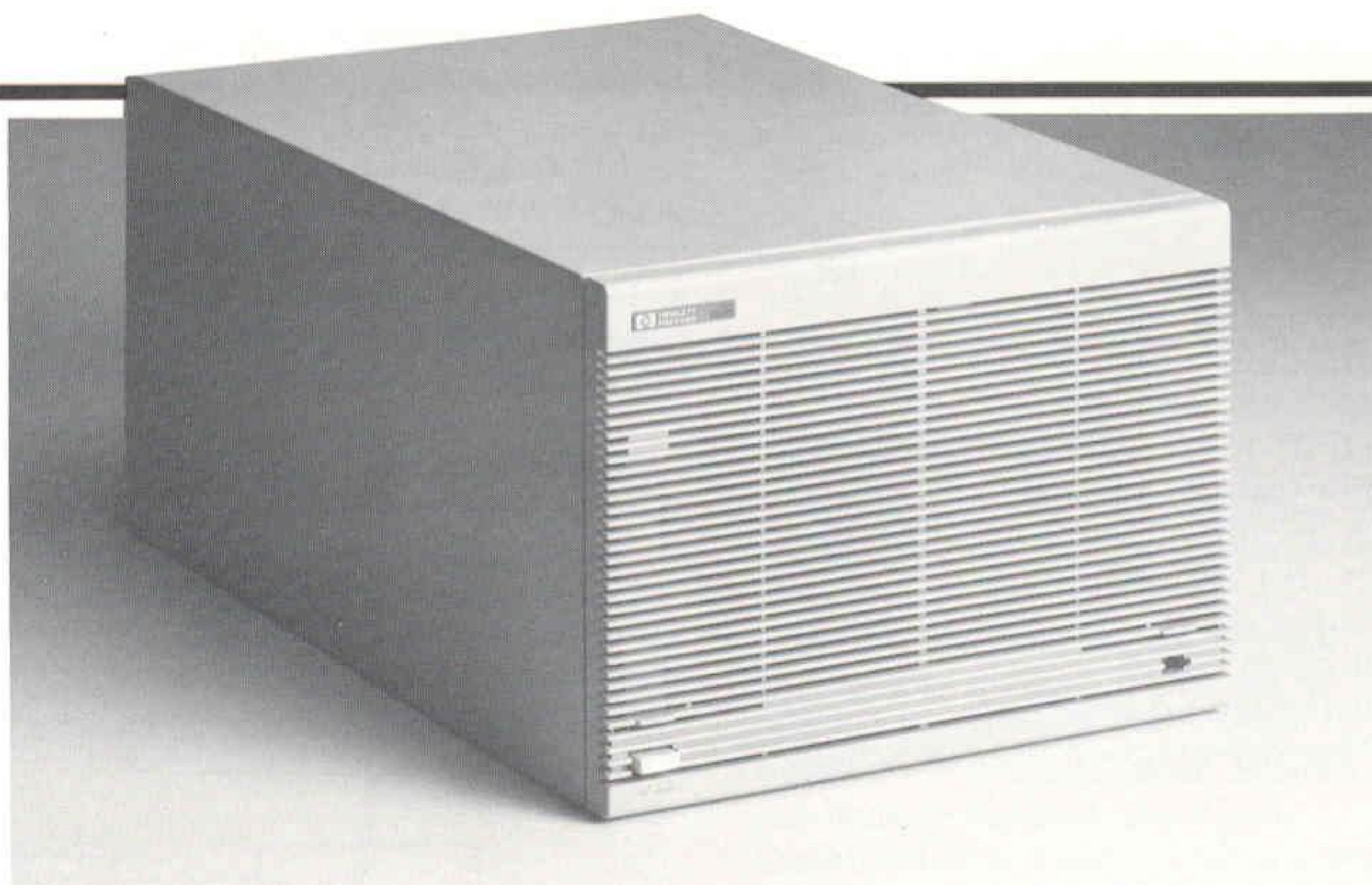
Product Description

The HP 3000 Series 935 is a high performance member of the HP 3000 family of business computers. Since it is compatible with the other HP 3000 systems, a multitude of business solutions is available for the Series 935—making it the ideal computing system for medium-sized businesses and large departments.

The Series 935 is based upon HP Precision Architecture, a reduced instruction set computer approach that provides increased power—at a lower cost than more complex designs. Utilizing sophisticated NMOS III Very Large Scale Integration (VLSI) circuit technology, the Series 935 delivers superminicomputer performance in a surprisingly small size. The hardware performance of the Series 935 combines with the enhanced MPE XL operating system to provide excellent throughput and industry leading price/performance—in both transaction processing and batch data processing environments.

An entire Series 935 system can be contained in a compact, attractive cabinet.

The Series 935 is highly reliable due to its low number of parts, and does not require a special computer room environment. And it is backed by the high standards of quality and support for which the HP 3000 is known.



Features

- HP Precision Architecture
- 48-bit virtual addressing
- 128 Kbytes high-speed CPU cache
- Advanced instruction pipelining techniques
- 48 Mbytes ECC memory standard, expandable to 96 Mbytes
- High Performance Floating Point Coprocessor
- 4096-entry Translation Lookaside Buffer for virtual-to-physical address translations
- Battery-backup, auto restart
- I/O bus
- Low power and cooling requirements
- Support for up to 240 users
- Terminal connection via IEEE 802.3 Local Area Network
- MPE XL operating system
- Network and relational database management systems standard

Advanced technologies

HP Precision Architecture

The Series 935 uses HP Precision Architecture (HPPA) to achieve high performance and reliability at a low cost. HPPA is based on the concept of Reduced Instruction Set Computing (RISC), a design approach that leads to greatly simplified computers, which are optimized to provide the highest performance for a given integrated circuit (IC) technology. In addition to offering higher performance, the inherent simplicity of HPPA means lower cost and higher reliability because machines can be implemented with fewer components.

At the core of HPPA is an instruction set containing 140 carefully selected, fixed-format instructions. Because the instruction set is simple, instructions can be hard-wired directly into the Central Processing Unit (CPU). This eliminates the need for microcode and

the necessity to decode complex instructions. HPPA utilizes a Load/Store design to reduce the number of relatively slow memory accesses, as most operations are performed register-to-register. To further enhance performance, optimizing compilers are used to schedule instructions and manage the instruction pipeline. With hardwired control, a Load/Store design, and optimizing compilers, one instruction is executed with virtually every clock cycle. Single cycle execution provides much of the performance benefit of HPPA over traditional architectures.

HPPA also incorporates many other features unrelated to RISC that greatly enhance its functionality. For example:

- Support for coprocessors (i.e., floating point)
- Extended addressing
- Memory-mapped I/O subsystem

System Organization

The processor communicates with memory and I/O via the Central Bus (CTB). The 10 MHz Central Bus provides a 32-bit data path, and can support data transfer rates of up to 22.3 Mbytes per second. The CTB is interfaced to a separate 16-bit wide Channel I/O Bus (CIB) via a CIB Adapter. The CIB supports I/O interfaces to peripheral devices and datacommunications links. An additional CIB adapter is included for use with an optional CIB Expander, providing additional I/O support.

The Series 935 Processor

The Series 935 CPU is entirely contained on a single VLSI chip, providing high uniprocessor performance. Using double-sided surface mount technology, the whole processor (including 128 Kbytes cache, the TLB, floating point chips, and more) is contained on one small printed circuit board.

Together with a second board containing two CIB adapters and the real-time clock, the system is a two-board set implemented with

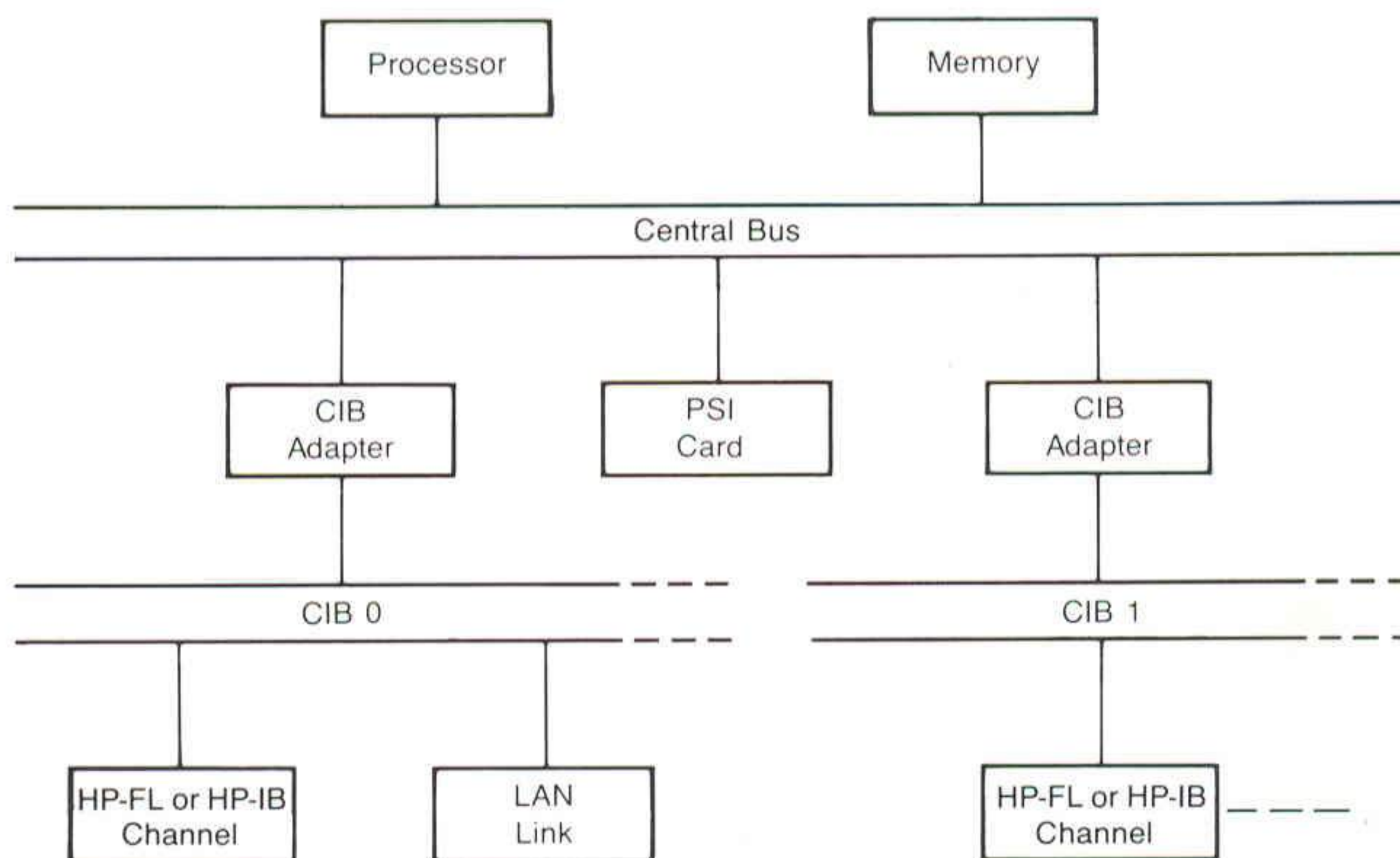


Figure 1 System Structure

NMOS III VLSI logic. With hard-wired control, the Series 935 is capable of executing one instruction every 66.7 nanosecond clock cycle. Separate Instruction and Execution units facilitate pipelining and allow for efficient, parallel use of processor resources.

Caches

The cache is a high-speed buffer for the CPU that minimizes the number of relatively slow transactions with main memory. The Series 935 uses a 128-Kbyte, high-speed, integrated CPU cache for data and instructions. The cache uses a write-to-management scheme, is two-way associative, and is organized in two sets of 2048 cache lines, with 32 bytes per cache line. Data modified in the cache is written to main memory only when the processor requires

other data to be in that cache location, or when a Direct Memory Access (DMA) operation is performed within that data area, or upon a power failure.

Instruction Pipelining

The Series 935 is pipelined at the instruction level, such that three instructions can be operated on simultaneously. The instruction pipeline consists of three 66.7 nanosecond stages. During the first stage, the instruction is fetched from the I-Cache and is decoded.

The specified function or calculation is performed during the second stage, and in the third stage the result of the calculation is saved to a CPU general purpose register. Excepting penalties for cache misses, etc., the net effect is that one instruction completes with every 66.7 nanosecond CPU cycle.

Floating Point Coprocessor

Single-precision and double-precision floating point calculations are performed by a Floating Point Coprocessor on the system board. The coprocessor significantly decreases the time required to perform floating point calculations. The Floating Point Coprocessor and the CPU can operate in parallel, thus allowing for increased performance in applications that utilize floating point.

Virtual Memory Management

Virtual Addresses on the Series 935 are 48 bits in length, ensuring sufficient expandability to meet evolving software needs. Virtual Memory is divided into a set of 65,536 spaces, with each space being 4 Gbytes in length. Spaces are further divided into fixed length 2-Kbyte pages, with a given page holding either data, code, or both. A single data structure can be up to 1 Gbyte, and code can span multiple spaces. This virtual memory scheme can accommodate virtual memory of more than 260,000 Gbytes.

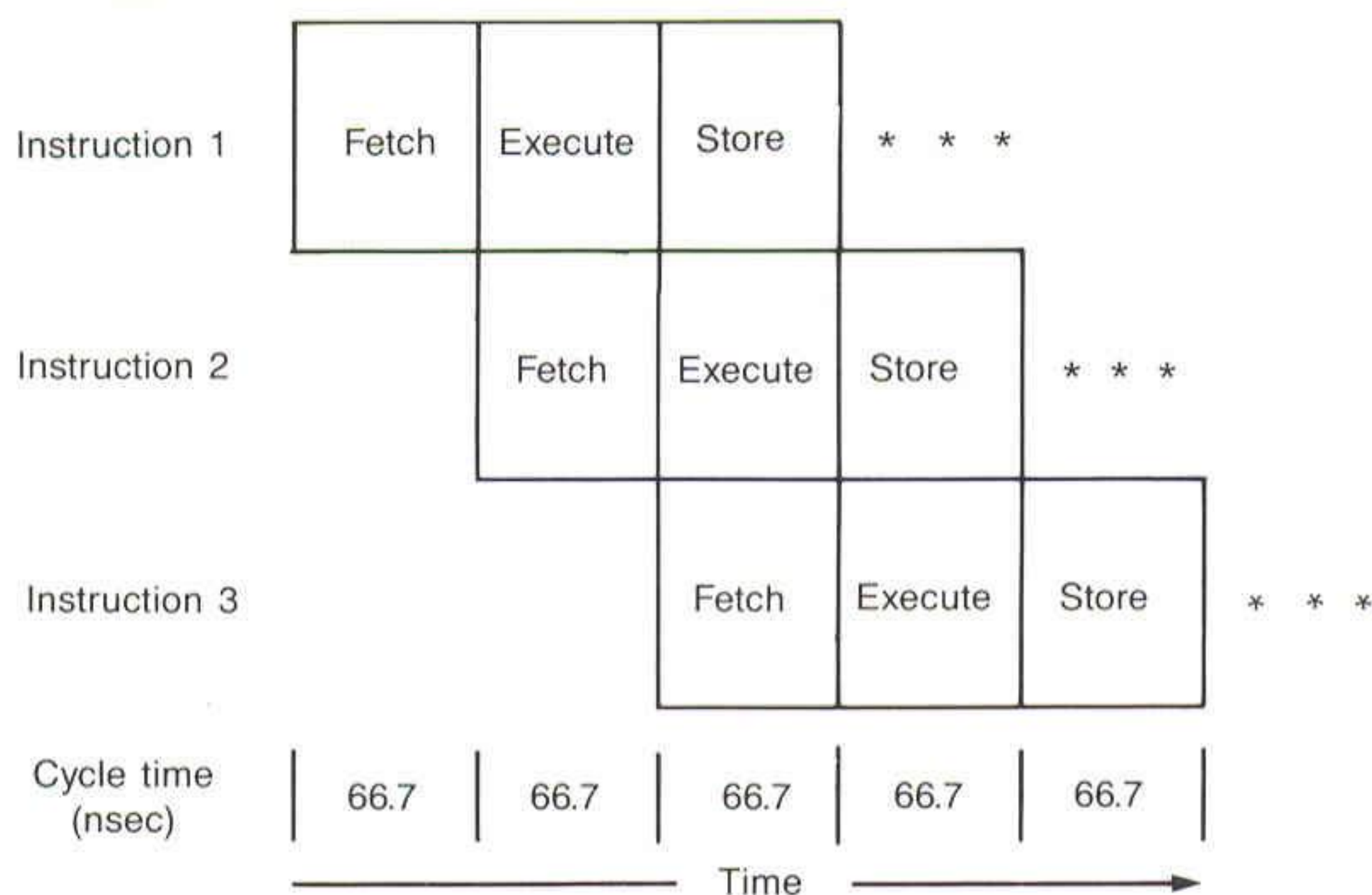


Figure 2 Instruction Pipelining

Virtual Address Translation

Virtual-to-Physical address translation is done by Translation Lookaside Buffers (TLBs), which cache recently accessed virtual page translations and convert the 48-bit virtual address into a 28-bit real address. The Series 935 TLB holds translations for 4096 virtual pages and is split into a 2048-entry instruction TLB and a 2048-entry data TLB. Page-level access protection is provided on the Series 935, and the TLB hardware supports protection mechanisms to ensure that the currently executing process has sufficient authorization to perform the requested data, code, or I/O access.

Memory Subsystem

The Series 935 supports 48 Mbytes of main memory standard and is expandable to 96 Mbytes in 8-Mbyte and 16-Mbyte increments. The memory subsystem uses 1 M-bit, Nibble-mode Dynamic RAMs. Main memory has battery backup to ensure that information is maintained for a minimum of 15 minutes in the event of an interruption in AC power. This allows the operating system to be automatically restarted and processing to continue without data loss, upon resumption of power.

The internal memory word size is 72 bits, with 64 data bits plus eight bits for error detection and correction. Single-bit memory errors are automatically corrected, with automatic detection of all double-bit errors. The ECC memory assures high memory performance and availability.

I/O Subsystem

I/O Buses

The Channel I/O Bus (CIB) supports up to seven cards for interfacing peripheral devices and providing data communications functions. Two CIB adapters and one 16-bit, 5-Mbyte bandwidth CIB are included, and an optional CIB Expander can be added for a total of 12 card slots. Each CIB Adapter provides DMA functions and supports up to a 5 Mbytes/second data throughput capability. The CIB adapter directly interfaces with the Central Bus (CTB). The CTB runs synchronously with a 10 MHz clock, and can support data transfer rates of up to 22.3 Mbytes/second.

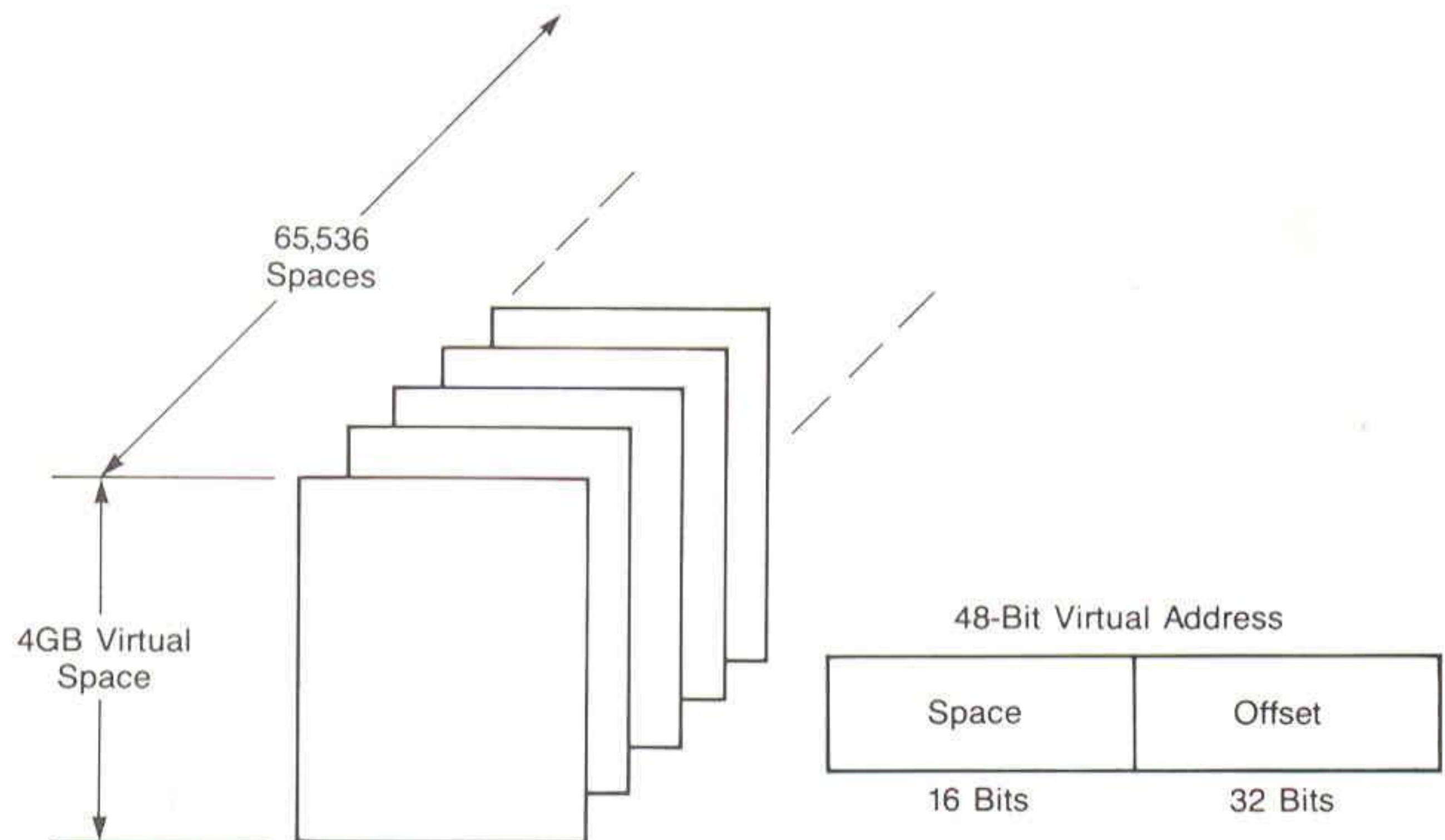


Figure 3 Virtual Memory Organization

Memory-Mapped I/O

Input/Output operations are initiated and controlled via a memory-mapped I/O scheme, such that the processor only needs to access reserved virtual or physical memory locations to control I/O operations. Memory-Mapped I/O allows for streamlined I/O operations and thus increases system performance in I/O intensive applications.

Peripheral Connections

Disks, tapes, and printers are connected via an HP-IB Channel which supports the 8-bit wide, IEEE-4888 standard Hewlett-Packard Interface Bus (HP-IB). Each HP-IB card supports up to six peripheral devices.

Workstation and Serial Printer Connection

Connections for workstations, serial printers, and other serial devices are provided via one or more Distributed Terminal Controllers (DTCs), which are distributed over an IEEE 802.3 standard Local Area Network (LAN). This flexible connection scheme allows DTCs to be situated in the department that they service, saving the cost and effort of running cables from each workstation back to the processor. Each DTC can support up to 48 direct connect ports, or 36 modem ports, or a combination of the two. Both RS-232 and RS-422 interfaces are supported.

System Packaging

The Series 935 is available in two, compact, attractive cabinets: a .53 meter and a 1.6 meter cabinet. The .53 meter cabinet is capable of holding the SPU and the optional Expander. The 1.6 meter cabinet has been uniquely designed to hold an entire modular system in a very small amount of space, maximizing the efficiency of office or computer room space. It is capable of holding the SPU, one DTC, a magnetic tape drive, and two disc drives. If desired, the Expander can be installed in the cabinet in place of the second disc drive.

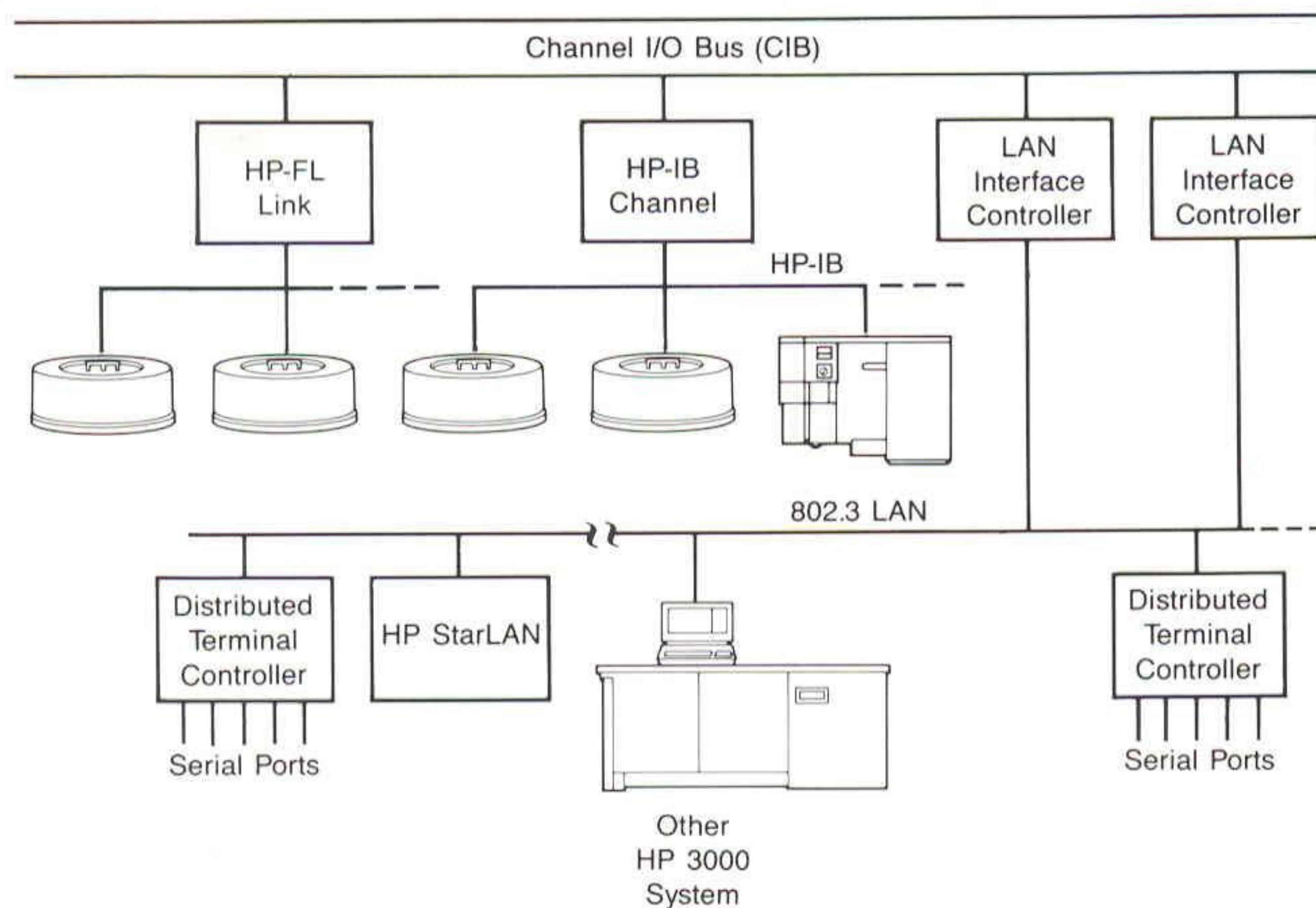


Figure 4 I/O Attachments

System-to-System Datacommunications

NS3000/XL and LAN Link/XL provide Virtual Terminal, Network File Transfer, Remote File and Database Access, Network Interprocess Communication, and Remote Process Management between HP 3000s on an IEEE 802.3 LAN. These same capabilities for remote communications are currently provided via an MPE V HP 3000 system. SNA IMF, SNA NRJE, and SNA Link provide HP 3000 to IBM system communications.

Environmental Specifications

Regulatory Compliance	Safety compliant with UL 478, CSA 220, and IEC 380/435.
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Electromagnetic Interference	Complies with FCC Rules and Regulations, Part 15, Subpart J, as a Class A computing device. Manufacturer's declaration verifies VDE level B. Registered as a VCCI Class I product.
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AC Power Input Voltage/Frequency:		
Range	Tolerance	Maximum Current
100V	90-110 VAC, 48-66 Hz	9.5A
120V	108-132 VAC, 48-66 Hz	8.0A
240V	180-264 VAC, 48-66 Hz	5.3A

Power Consumption:	600 Watts, 2034 BTU/hr.
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Physical Dimensions

Height:	234 mm (9.21 in.)
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Width:	325 mm (12.8 in.)
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Depth:	500 mm (19.7 in.)
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Weight:	23 kg (51 lbs)
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Operating Temperature:	0 to 55 degrees C (32 to 131 degrees F)
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Non-operating Temperature:	-40 to 71 degrees C; (-40 to 159 degrees F)
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Relative Humidity:	15% to 95% at 0-40 degrees C, non-condensing
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Altitude (operating):	To 4.6 km (15,000 feet)
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(non-operating):	To 15.3 km (50,000 feet)
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Battery Backup Time, Minimum:	15 minutes
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Acoustics:	5.0 bels (A) sound power
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Ventilation:	Forced air cooling, air flows from front to back.
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System Software

Listed below are software products currently available for the HP 3000 Series 935 as of MPE XL Release 1.1. This list will be expanded over time as development and testing of additional software products continue. Check with your local Sales Representative for more information.

Operating System

MPE XL

Datacommunications

NS3000/XL
LAN Link/XL
SNA IMF
SNA NRJE
SNA Link

Utilities

EDIT/V
FCOPY/XL
SORT-MERGE/XL

Office Services

HP DeskManager
HP/Spell/V
HP AdvancePrint
HP Curator
HP TDP/V

Languages

COBOL II/V
COBOL II/XL
HP Pascal/V
HP Pascal/XL
HP FORTRAN 66/V
HP FORTRAN 77/V
HP FORTRAN 77/XL

HP Business BASIC/V
HP BASIC/V
SPL/V
RPG/V
HP C/XL

Information Management

ALLBASE/XL
TurboIMAGE/XL
Visor/XL
TurboIMAGE DBchange/V
HP System Dictionary/XL
Inform/V
Report/V
HP Toolset/XL
Information Access/XL

Query/V
Transact/V
Transact/XL
VPLUS/V
KSAM/V
Dictionary/V
BRW/V
BRW/XL

Application Software

A wide range of solutions available for the HP 3000 systems, including application areas such as manufacturing, financial, and information management. Your Sales Representative can provide more information that is specific to your needs.

Supported Peripherals

Listed below are peripheral devices currently available for the HP 3000 Series 935 as of MPE Release 1.1. This list will be expanded over time as development and testing of additional peripherals continues. Check with your sales representative for more information.

Support Services

A wide range of hardware and software support services are available worldwide for all HP 3000 products. Contact your HP Sales Representative for details on available support services.

Ordering Information

The HP 3000 Series 935 SPU includes 48 Mbytes main memory, one CIB, two CIB adapters, one LAN interface, a console connection, and two HP-IB channels. Return credits are available when upgrading other HP 3000 systems to the Series 935. For more information, contact your local HP sales office.

Terminals

2392	Vectra PC
2393	Portable Plus
2397	Vectra CS
2394	HP Vectra ES, ES12
700/92	Touchscreen II PC
700/94	

Disc Drives

7937H/XP	7935H/XP
7933H/XP	7936H/XP
	7937FL

Tape Drives

7978A/B	7979A
7974A	7980A

Printers

2680	2934
2688	2563A/B
2566A/B	2564B
2565A	2567B
2686	LaserJet 2000

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